

1. Schematic Page Description :

Origins Schematic Ver :

01

SoC I2C table

Function	Channel	Read	Write
NA	I2C0	0x?	
PMIC	I2C1	0x?	0x?
Audio codec	I2C4		
Track Pad	I2C5		
EC	I2C6		

EC SMBus/I2C table

Function	Channel	Address
Battery/charger	SMB0	
NA	SMB1	
PCH	I2C1	
NA	I2C2	
Thermal	I2C3	

USB3/2 port mapping

USB3 Port No#	Usage	USB2 Port No#	Usage
USB3P0	NA	USB2P0	NA
USB3P1	I/O	USB2P1	I/O(3.0)
USB3P2	I/O	USB2P2	I/O(3.0)
USB3P3	NA	USB2P3	CCD
		USB2P4	BT

PCIe port mapping

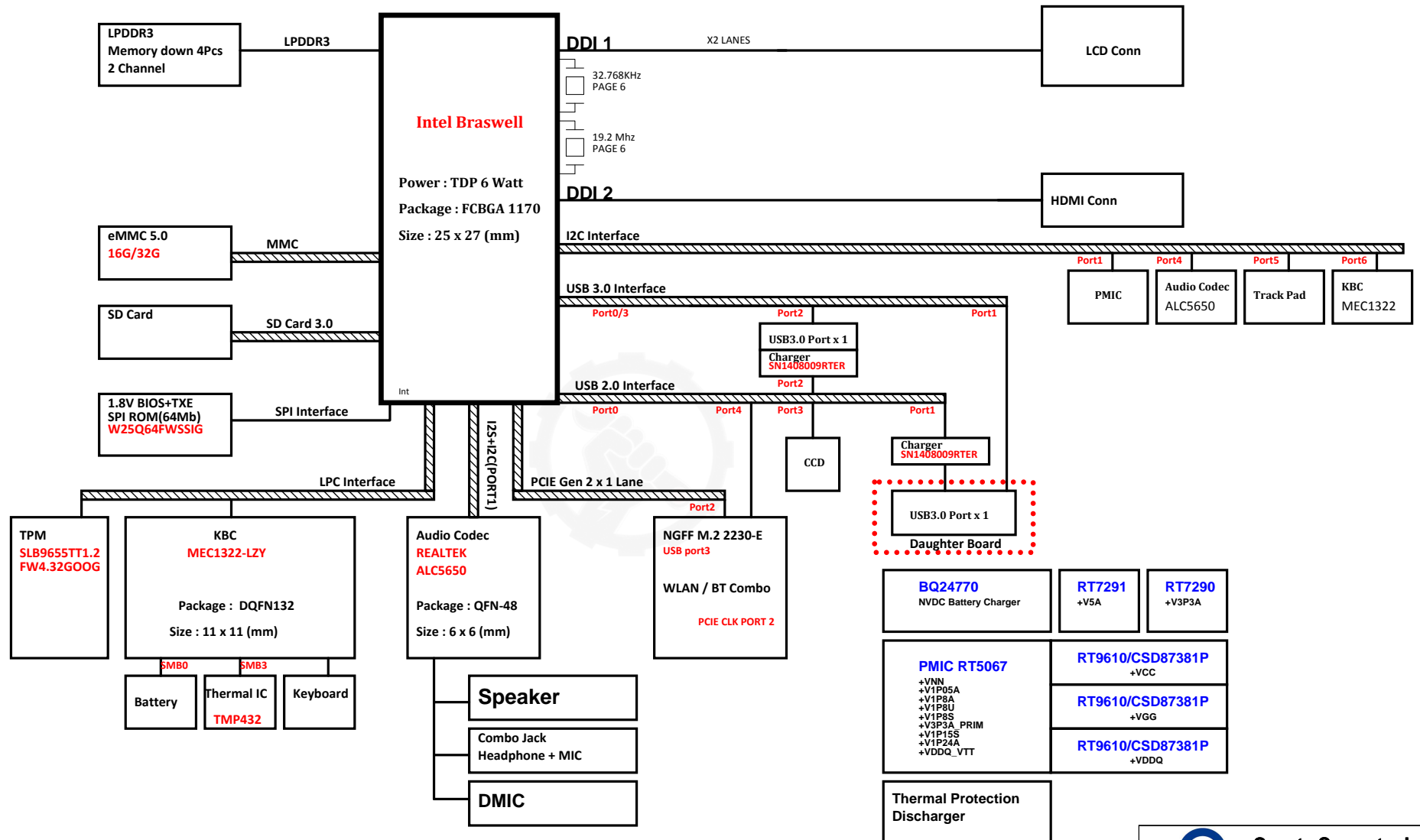
PCIe port No#	Usage	PCIe CLK#	Usage
PCIe_0	NA	PCIe_CLK0	NA
PCIe_1	NA	PCIe_CLK1	NA
PCIe_2	WLAN	PCIe_CLK2	WLAN
PCIe_3	NA	PCIe_CLK3	NA

Current sensor address

Function	Channel	Function	Channel
+VBATA	0x47	+VCC_OUT	0x40
+V5A	0x43	+VGG	0x44
+V3P3A	0x4B	+VNN	0x45
+V1P05A	0x46	+VDDQ_OUT	0x41
+V1P8A	0x49		

ZHM Chromebook

Intel Braswell Platform Block Diagram

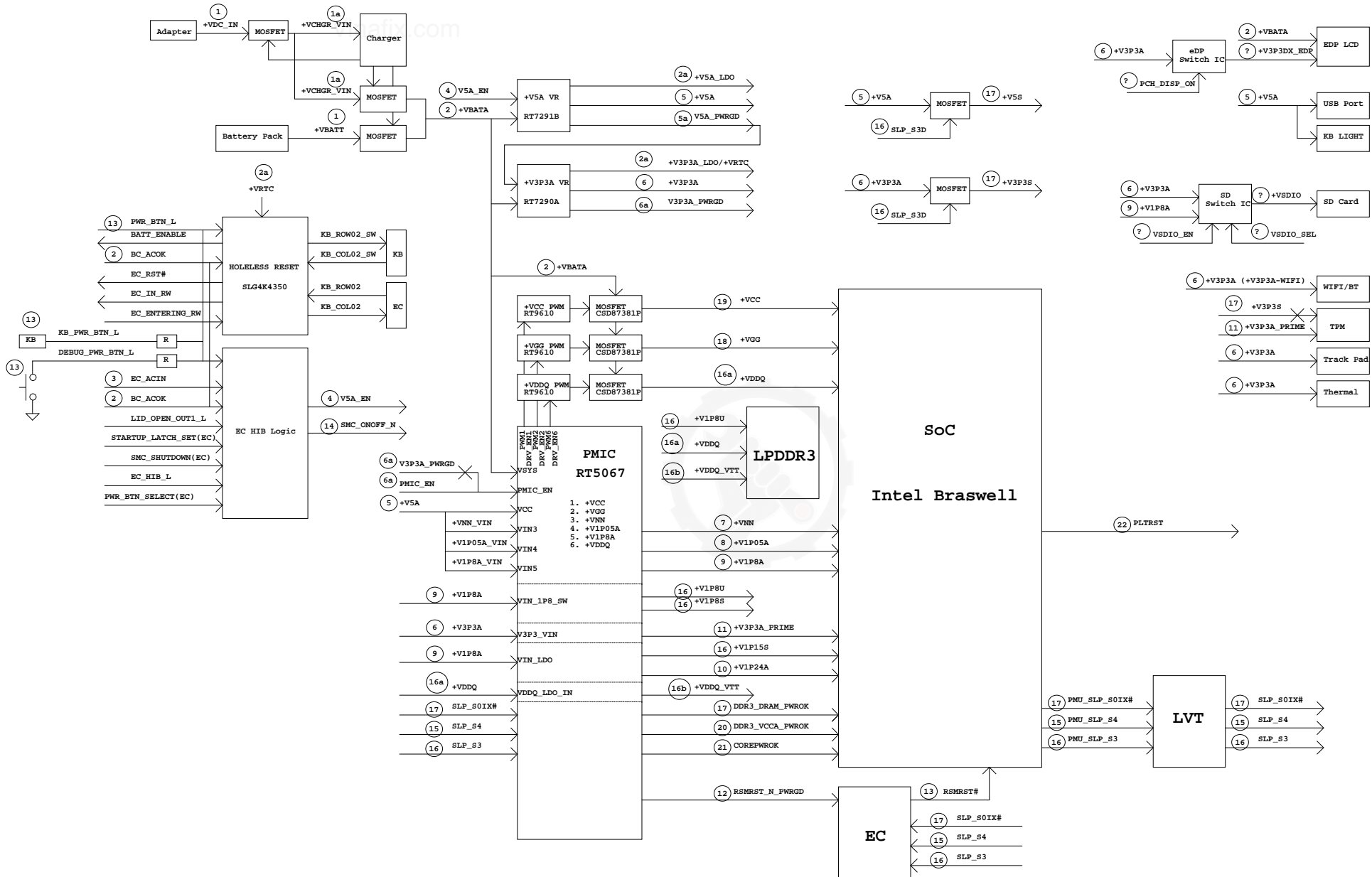


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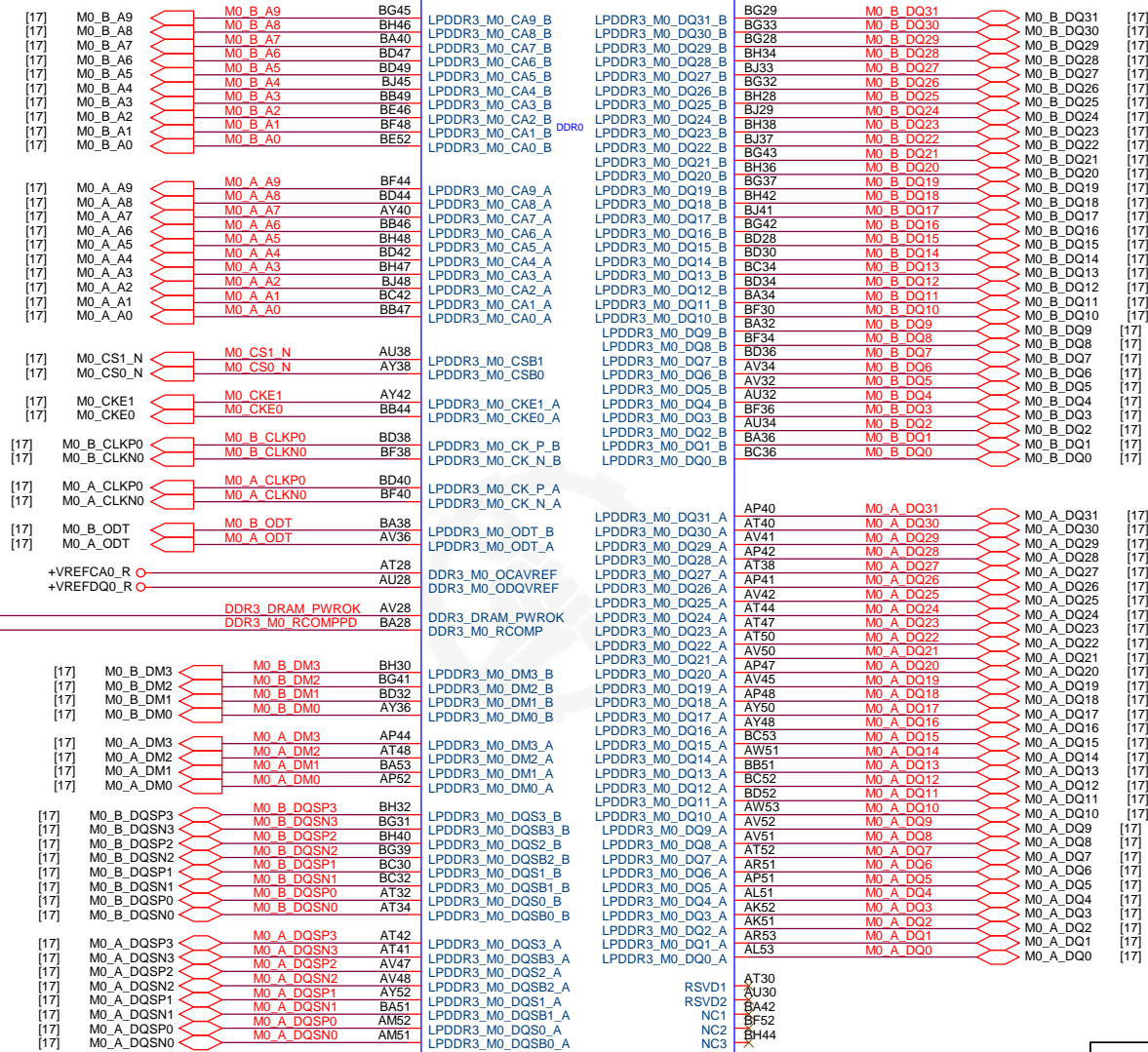


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BSW_MCP_EDS

U17A

?



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Size	Document Number	Rev
	BSW 1/10 (DDRA)	A1A
Date:	Monday, December 12, 2016	Sheet 6 of 44

BRASWELL - MEMORY LPDDR3 CHANNEL B

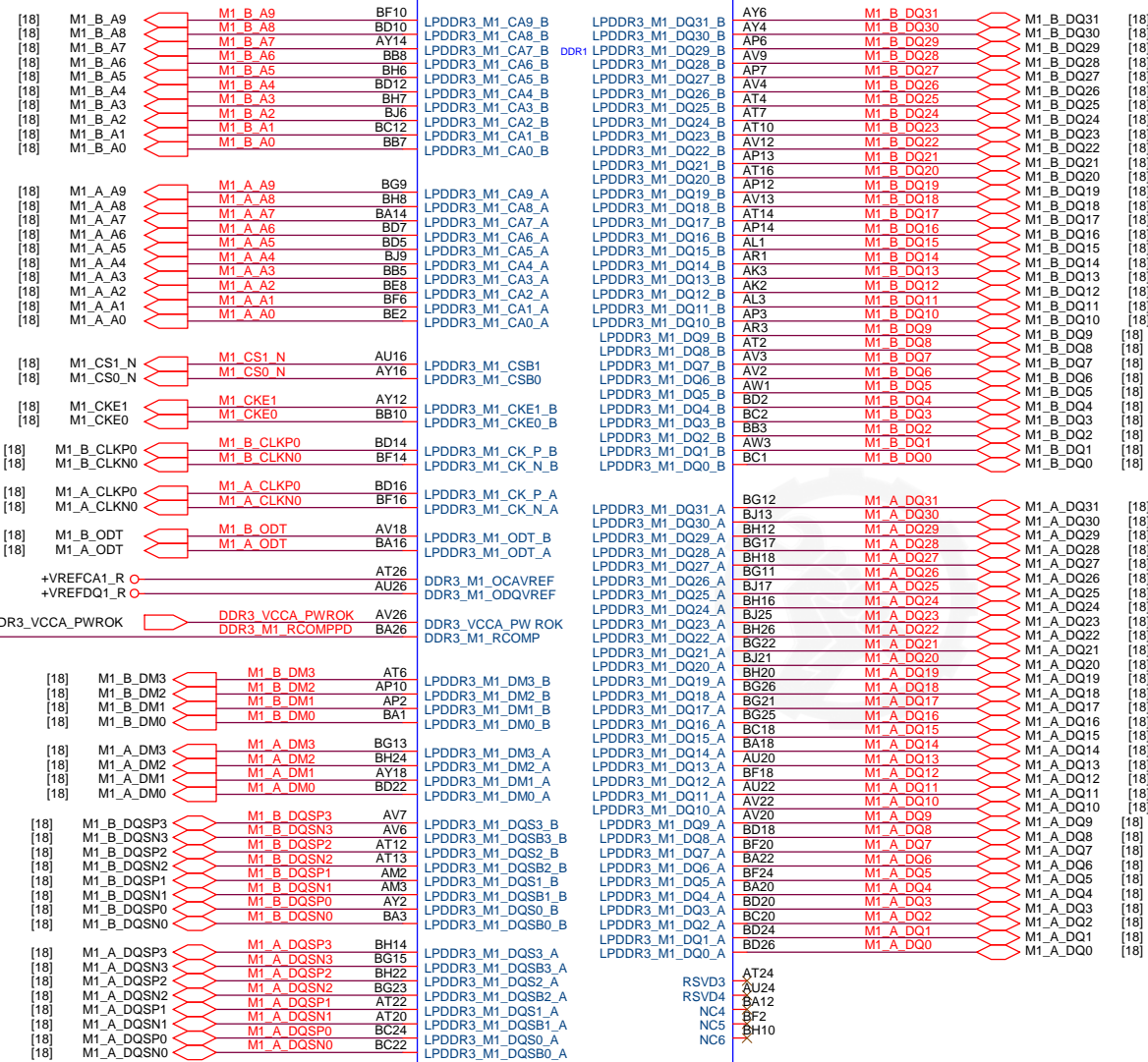
07

SoC (CPU)

BSW_MCP_EDS

U17B

7



2 OF 13

BSW_MCP_EDS
REV=1

7



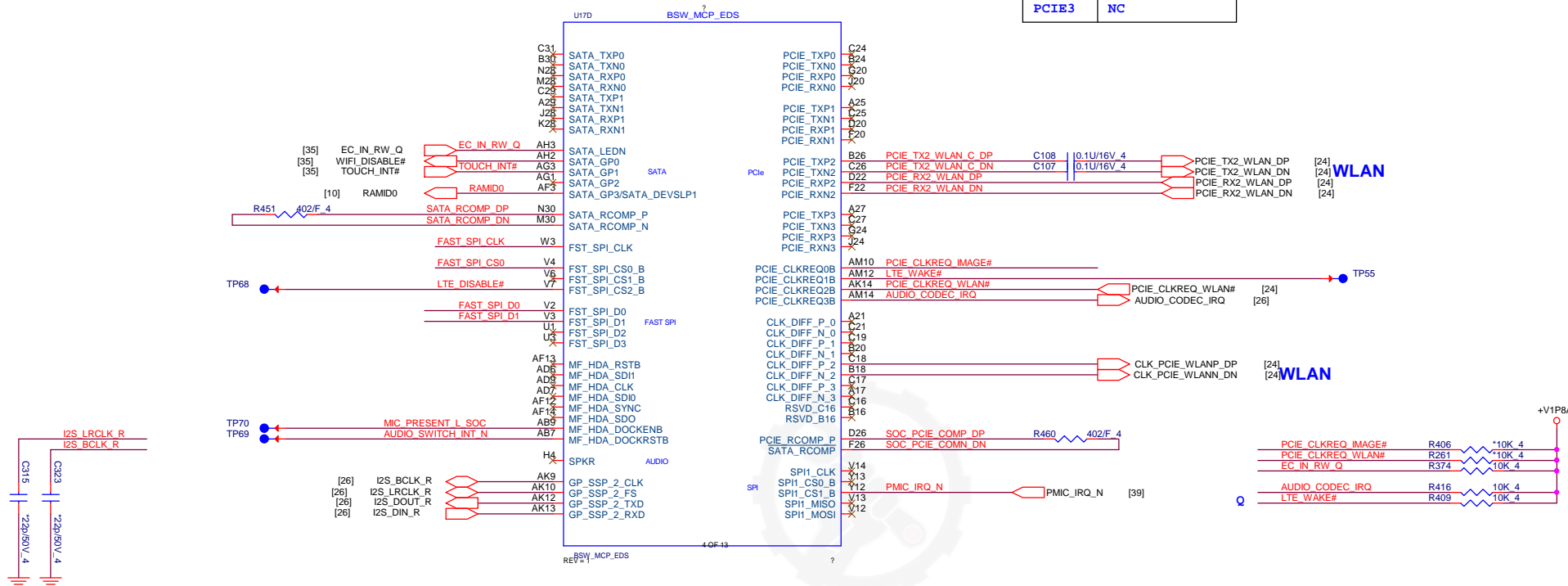
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PROJECT : ZHM

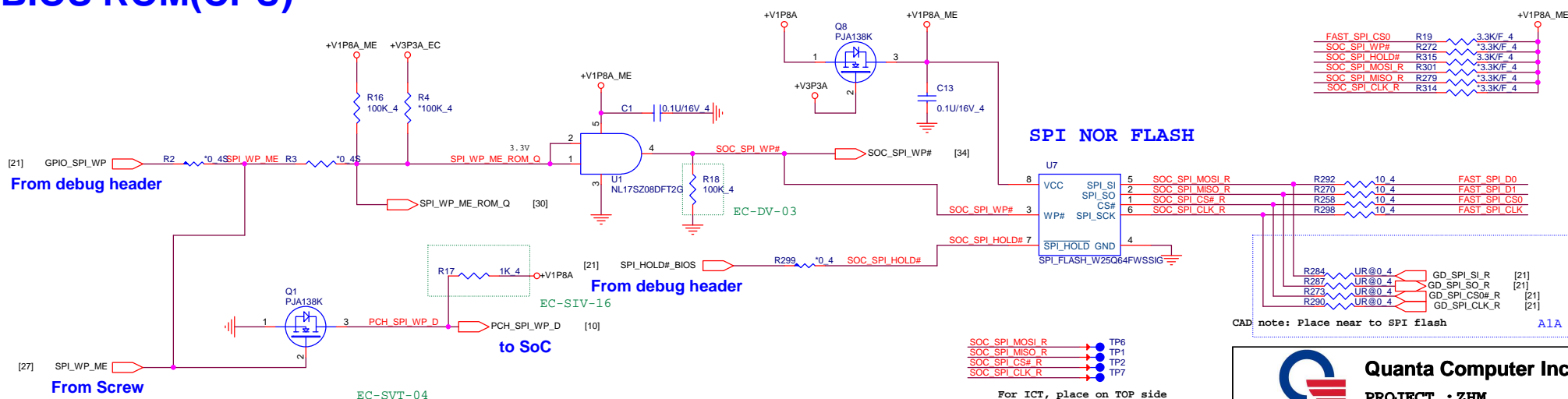
Size	Document Number	Rev
	BSW 2/10 (DDR3)	A1A
Date:	Monday, December 12, 2016	Sheet 7 of 44

09

PCIe MAPPING	
PCIE0	NC
PCIE1	NC
PCIE2	WIFI (StP)
PCIE3	NC



BIOS ROM(CPU)



CAD note: Place near to SPI flash



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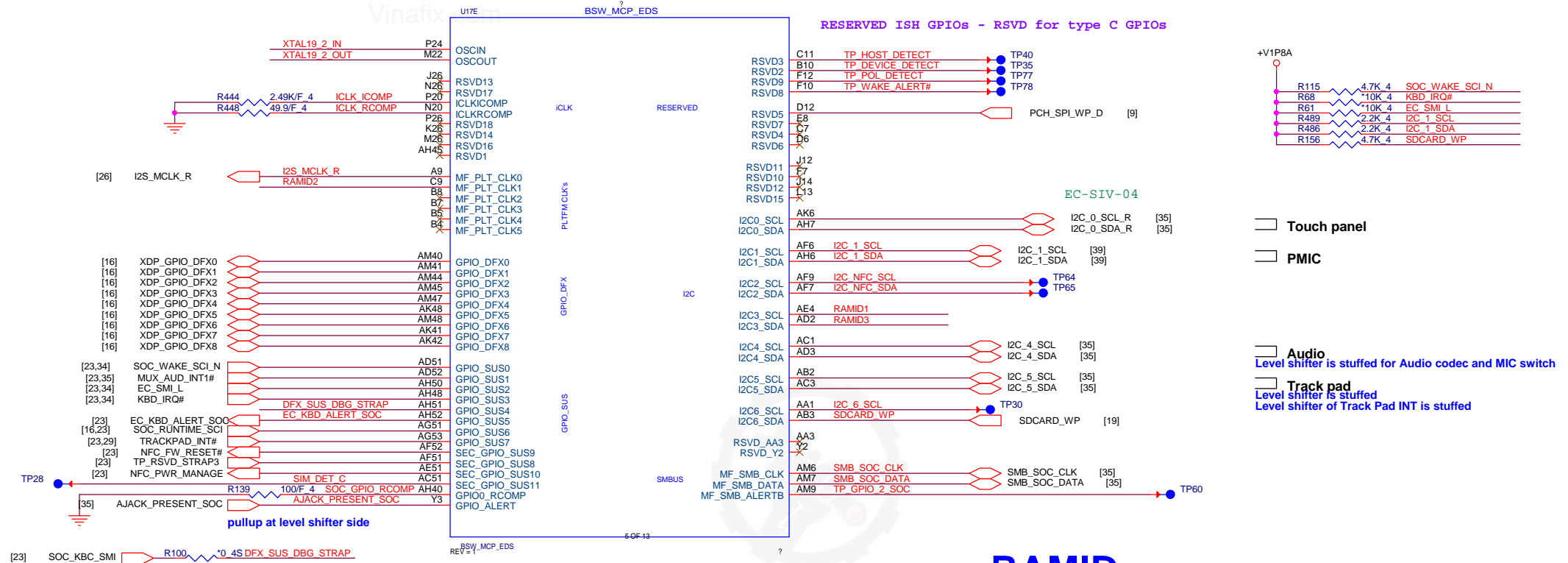
PROJECT : ZHM

BSW 4/10 (PCIE/SATA/SPI)

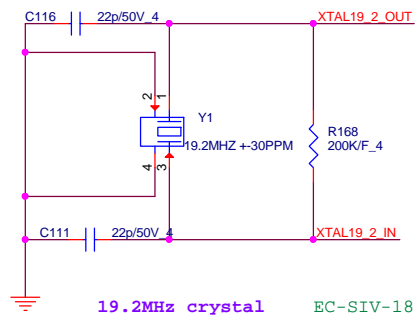
Date: Monday, December 12, 2016 Sheet 9 of 44

Rev
A1/

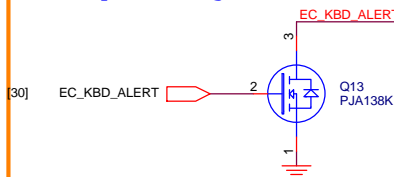
BRASWELL - I2C, XDP, SM BUS



19.2MHz X'tal

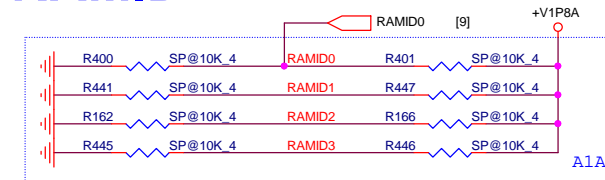


0312 added KBD_ALERT pin to notify SoC to lock ME FW
Keep reserving this feature in DVT build



Vender	RAM_ID3	RAM_ID[2..0]	Q PN	Mfr. PN	Freq.	Size	Total Size
Samsung	0 (1-CH)	000		K4E8E304EE-EGCF	1866MHz	4Gb	2GB
Hynix	0 (1-CH)	001		H9CCNNN8JTMLAR-NUD	1866MHz	4Gb	2GB
Micron	0 (1-CH)	010		MT52L256M32D1PF-107 WT:B	1866MHz	4Gb	2GB
Samsung	0 (1-CH)	011		K4E8E324EB-EGCF	1866MHz	4Gb	2GB
Micron	0 (1-CH)	100		EDF8132A3MA-JD-F-R	1866MHz	4Gb	2GB
Hynix	0 (1-CH)	101		H9CCNNN8JTBTLAR-NUD	1866MHz	4Gb	2GB
Samsung	1 (2-CH)	000		K4E8E304EE-EGCF	1866MHz	4Gb	4GB
Hynix	1 (2-CH)	001		H9CCNNN8JTMLAR-NUD	1866MHz	4Gb	4GB
Micron	1 (2-CH)	010		MT52L256M32D1PF-107 WT:B	1866MHz	4Gb	4GB
Samsung	1 (2-CH)	011		K4E8E324EB-EGCF	1866MHz	4Gb	4GB
Micron	1 (2-CH)	100		EDF8132A3MA-JD-F-R	1866MHz	4Gb	4GB
Hynix	1 (2-CH)	101		H9CCNNN8JTBTLAR-NUD	1866MHz	4Gb	4GB

RAMID



Samsung

Hynix

Micron

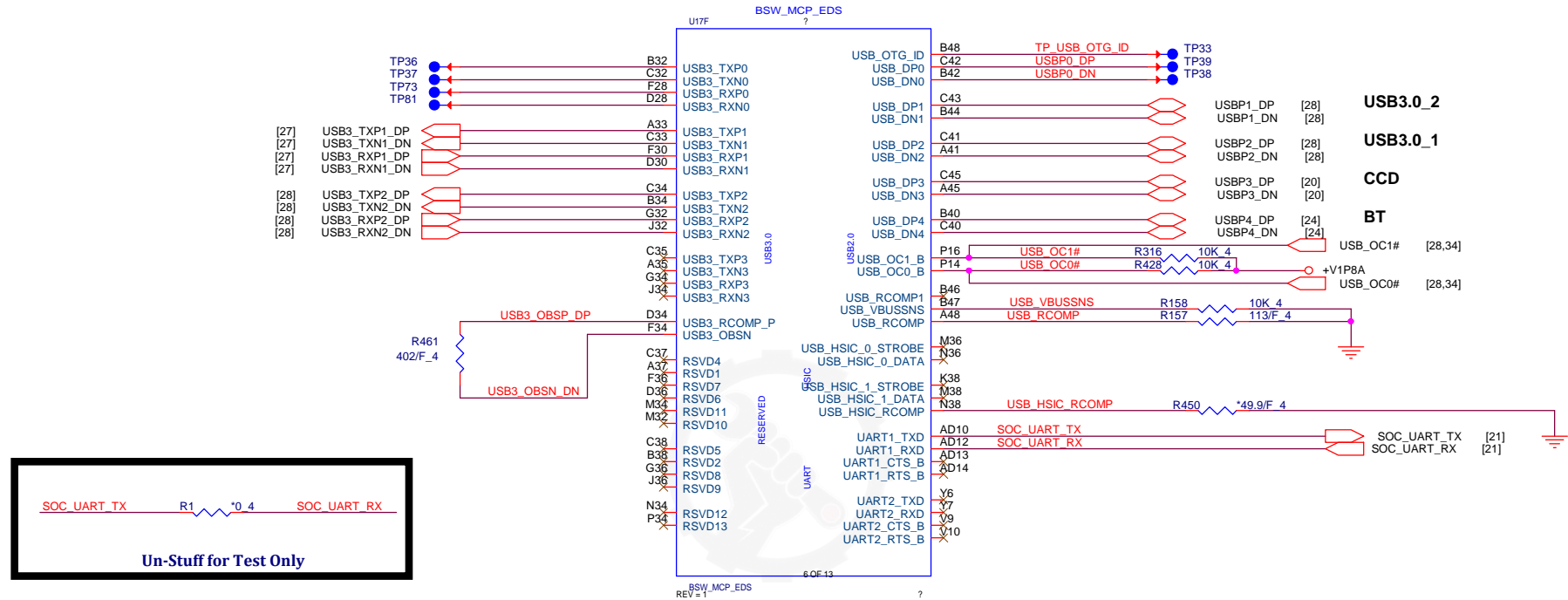
For BOM, place BOT side

BRASWELL - USB INTERFACE

11

SoC (CPU)

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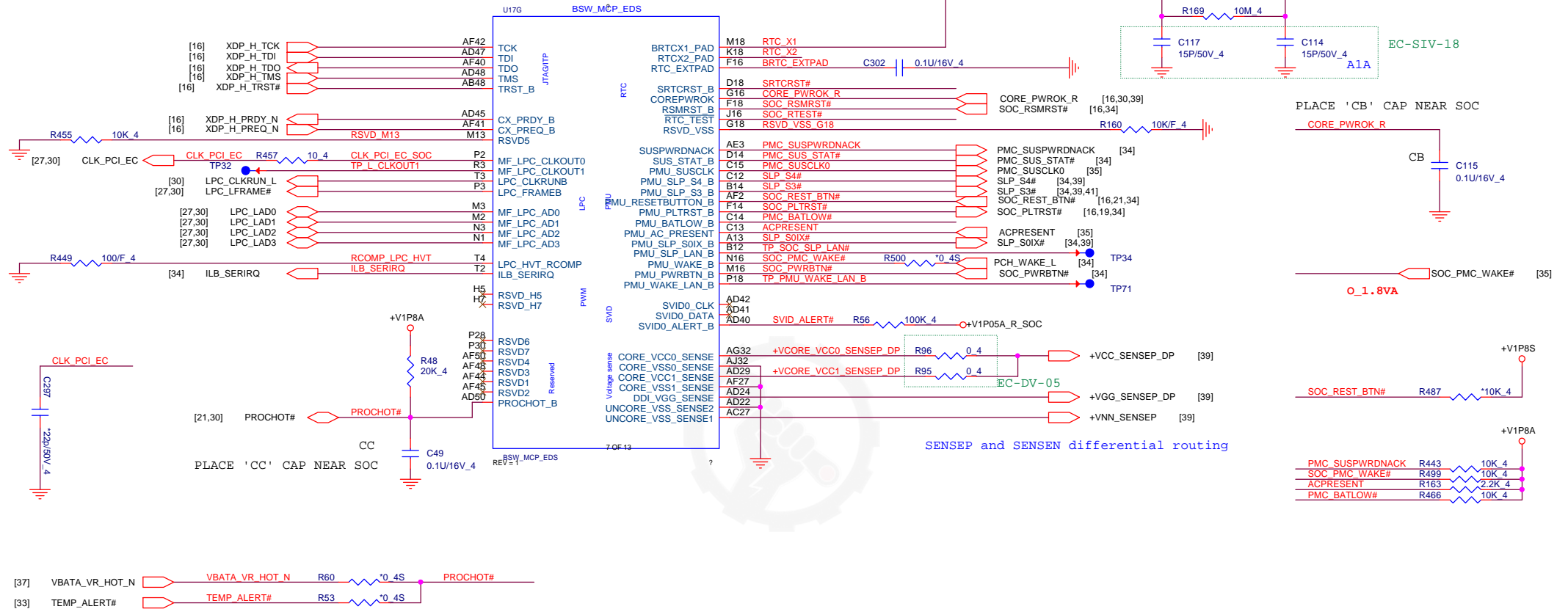
Size	Document Number	Rev
	BSW 6/10 (USB)	A1A
Date:	Monday, December 12, 2016	Sheet 11 of 44

BRASWELL - JTAG, LPC, THERMAL, PMU

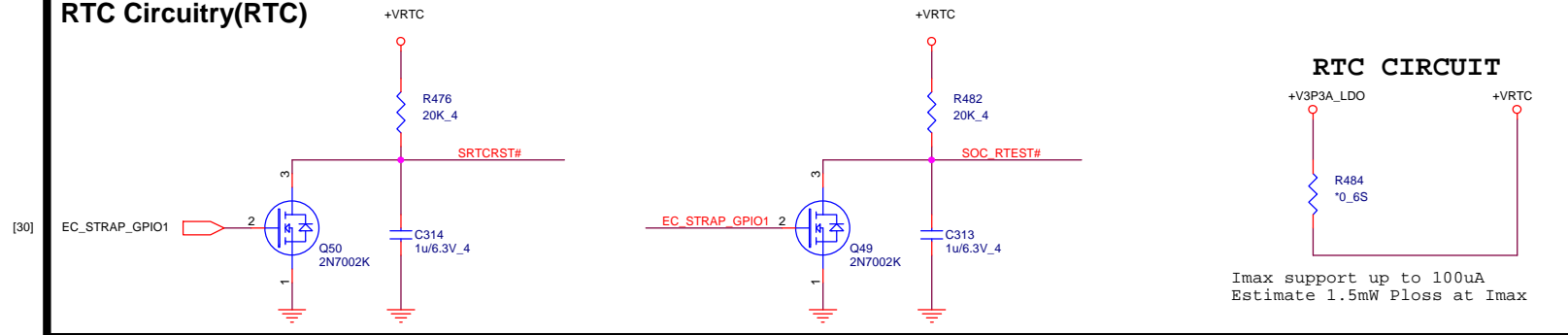
Vinafix.com

SoC (CPU)

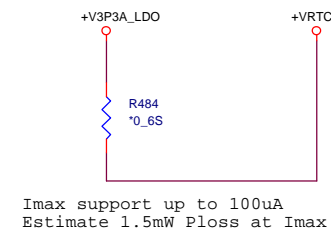
RTC 32.768KHz X'tal



RTC Circuitry(RTC)



RTC CIRCUIT



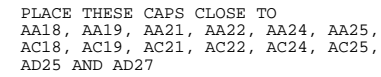
Imax support up to 100uA
Estimate 1.5mW Ploss at Imax



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Size	Document Number	Rev
	BSW 7/10 (JTAG/LPC/PMU)	A1A
Date:	Monday, December 12, 2016	Sheet 12 of 44



PLACE THESE CAPS CLOSE TO
V33, AA32, AA33, AA35, AA36,
AC32, Y30, Y32, Y33 AND Y35

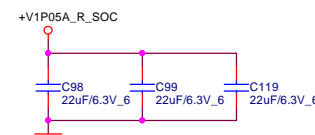
PLACE THIS CAP CLOSE TO V19 AND V18

PLACE THESE CAPS CLOSE TO
AM21, AM33, AM22, AN22, AN32
AND AM32

PLACE THESE CAPS CLOSE TO
V22, V24, U24, U22, V27 AND U27

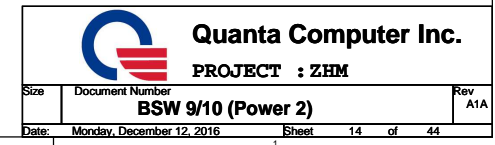
PLACE THIS
CAP CLOSE TO

PLACE THESE CAPS CLOSE TO U19



DUMMY CAPS. TO BE DELETED IN NEXT REVISION

CAD NOTE: PLACE CLOSE TO PIN AM21,
AM33, AM22, AN22, AN32 AND AM32 POWER PLANE

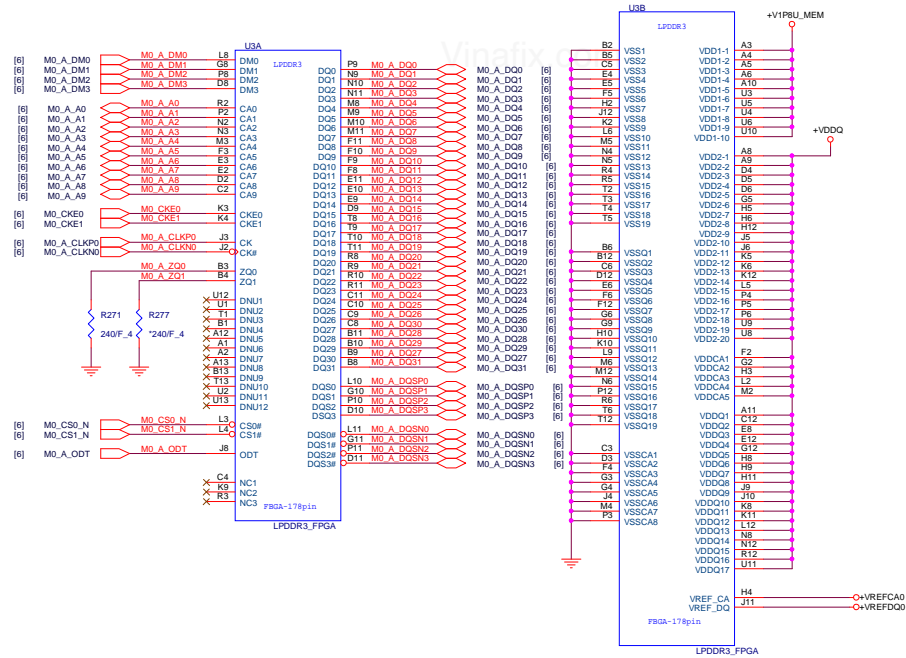


16

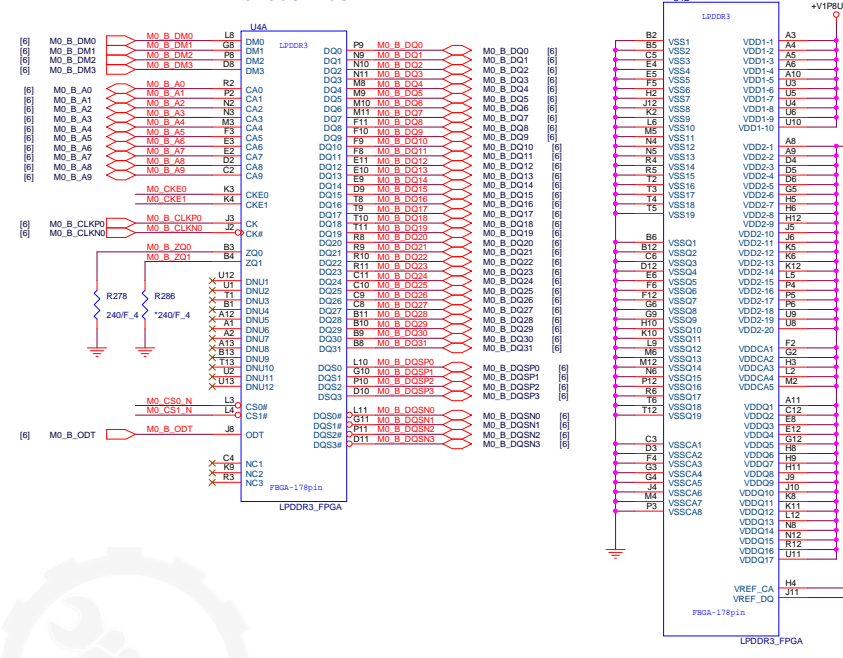
APS

EC-SIT-14

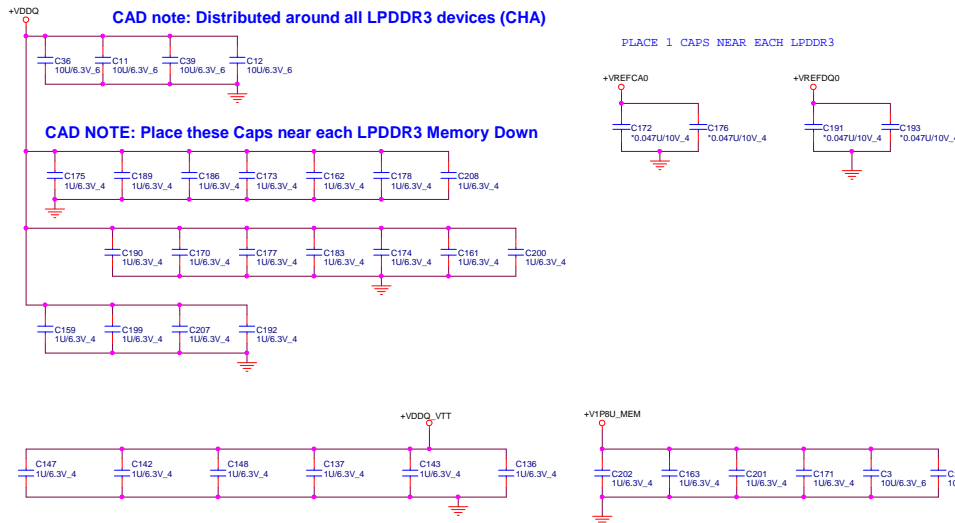
bit:0-31



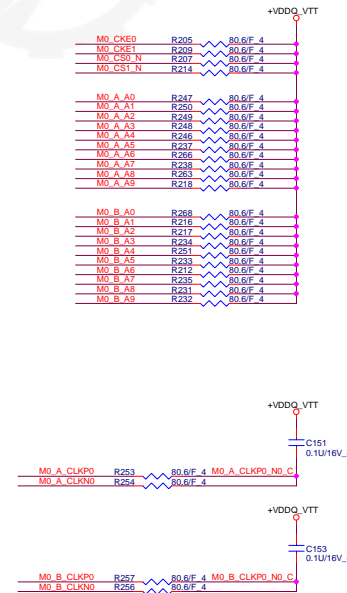
bit:32-63



DE-CAPS FOR MEMORY CHANNEL A

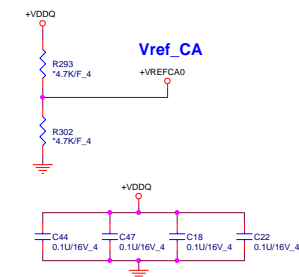


VTT TERMINATIONS



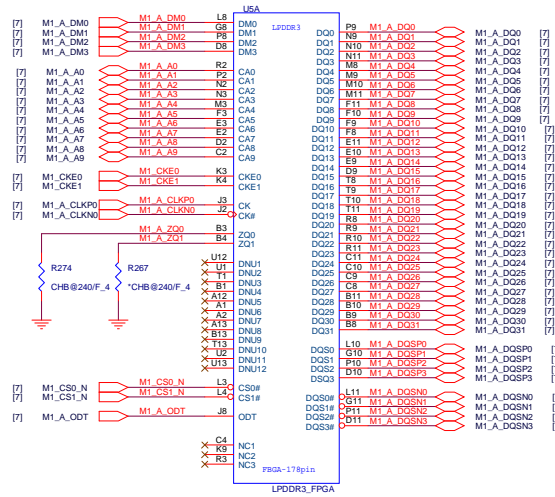
VOLTAGE MERGE

VREF_CA AND DQ CIRCUITS

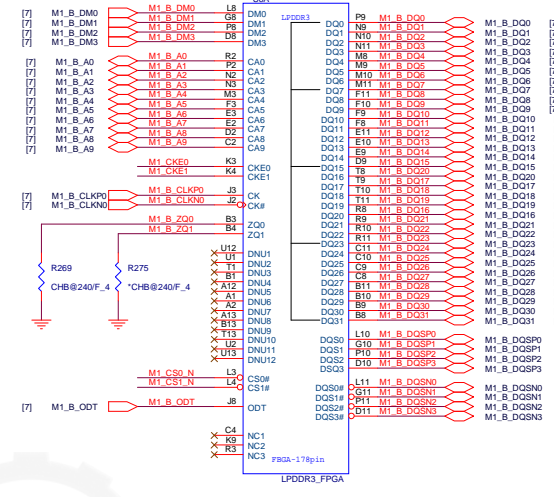


CHANNEL B:8Gb*2 LPDDR3

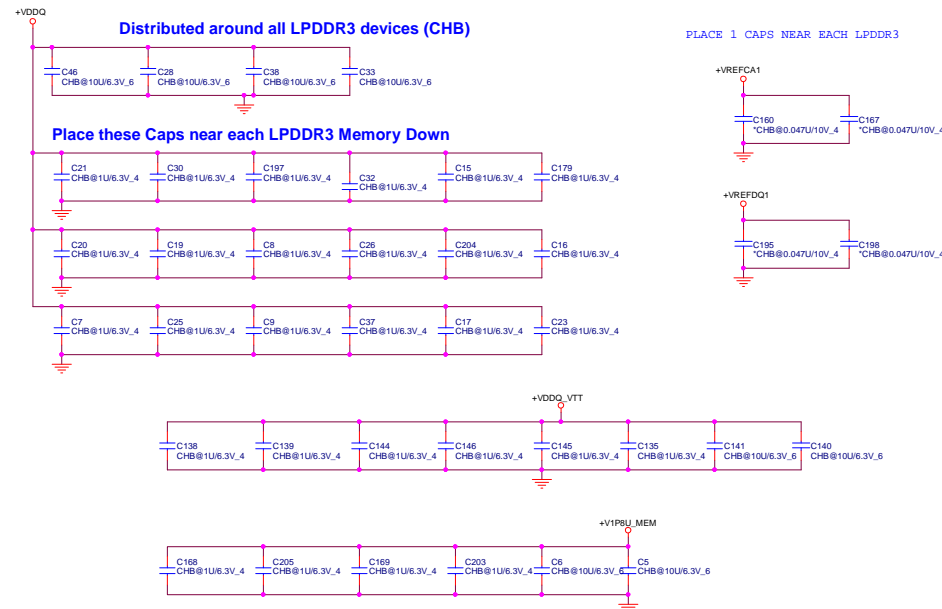
bit:0-31



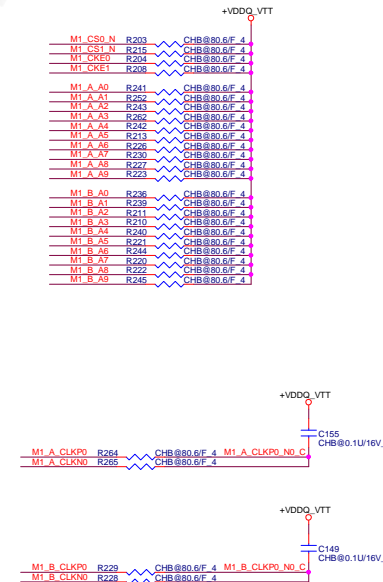
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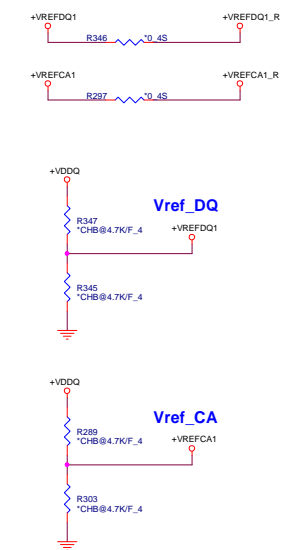
DE-CAPS FOR MEMORY CHANNEL B



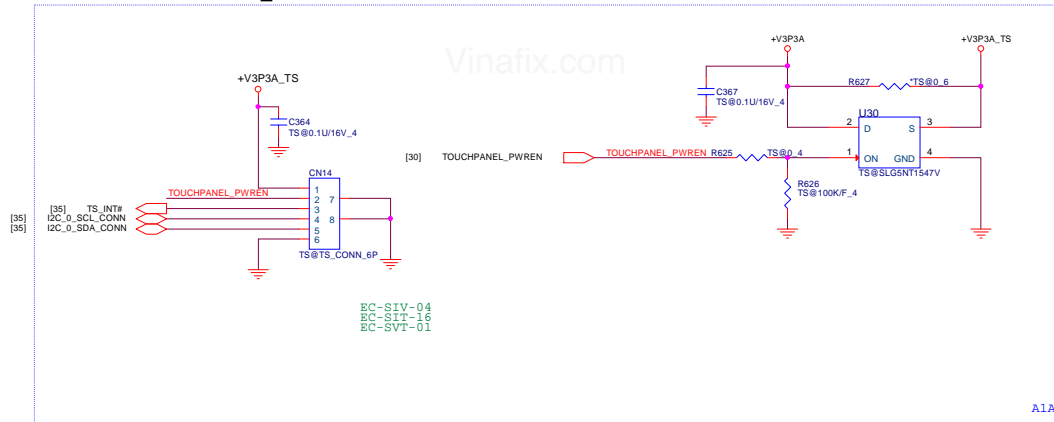
VTT TERMINATIONS



VREF_DQ CIRCUIT

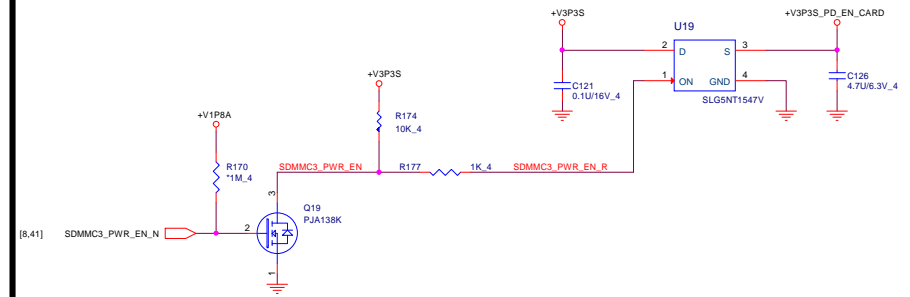


Touch panel connector



SD SLOT POWER SUPPLY

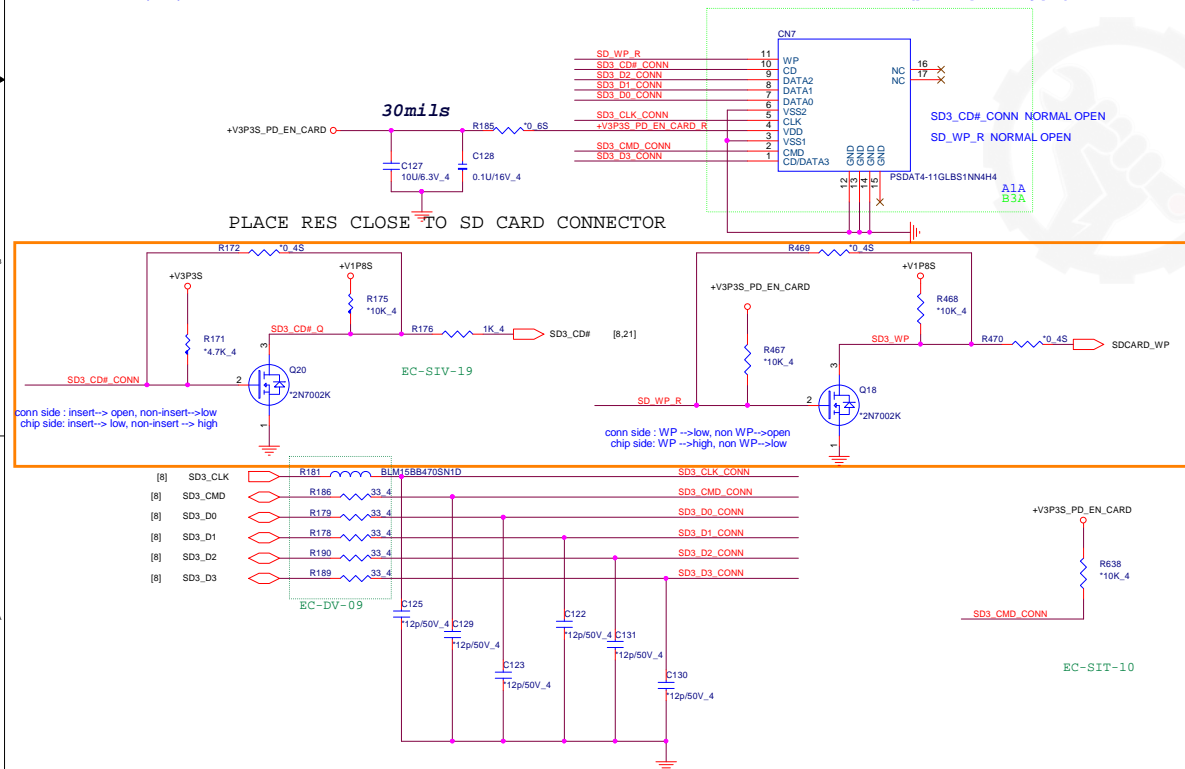
Card Reader (CRD)



SD SLOT/EMI

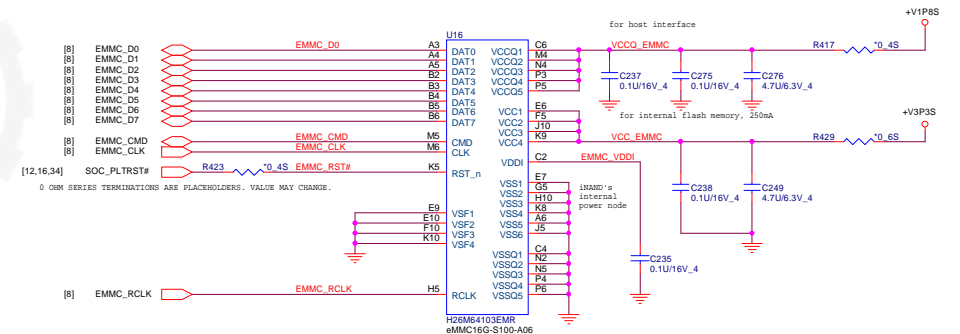
This is full size SD card (push-push type)

Card Reader (CRD)



eMMC (MMC)

eMMC



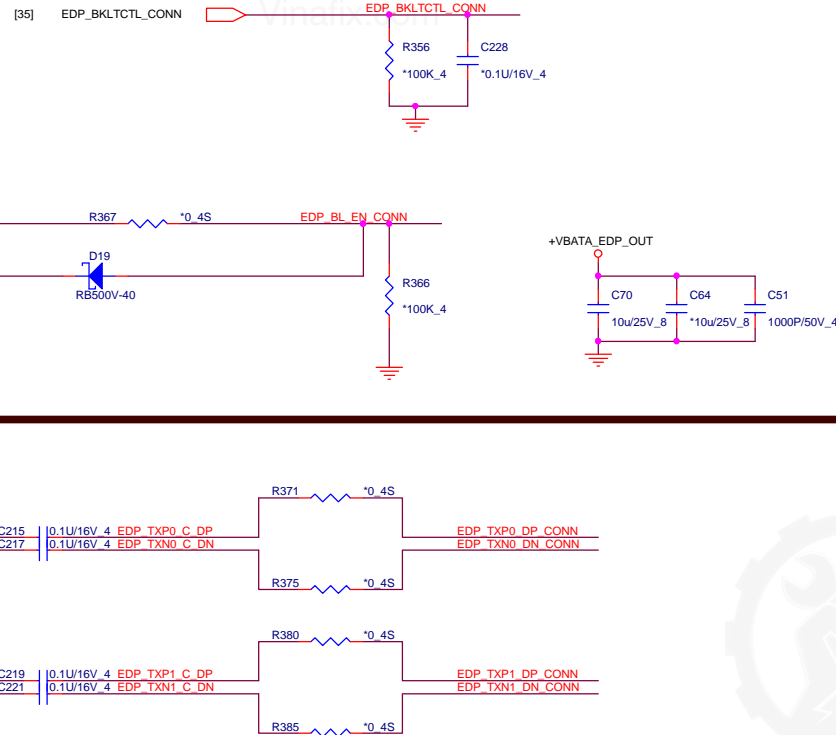
TP59 → EMMC_RCLK
 TP62 → EMMC_CLK
 TP66 → EMMC_CMD
 TP51 → EMMC_D0

16G
 Samsung-->KLMAG2WEMB-B031-AKE2RF-T505-- IC FLASH(153)KLMAG2WEMB-B031(FBGA)STNBSQ
 Hynix--> H26M52103FMR (0x03)--AR0ZHQRL000--PROG IC FLASH(153P)H26M52103FMR STNBSQ

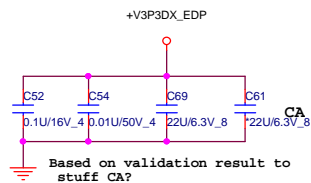
32G
 Samsung-->KLMAG4WEMB-B031-AKE3SZ-T500--IC FLASH(153)KLMAG4WEMB-B031(FBGA)STNBSQ
 Hynix--> H26M64103EMR (0x03)--AR0ZHQRL001--PROG IC FLASH(153P)H26M64103EMR STNBSQ

eDP PANEL CONTROL

LCD(LDS)

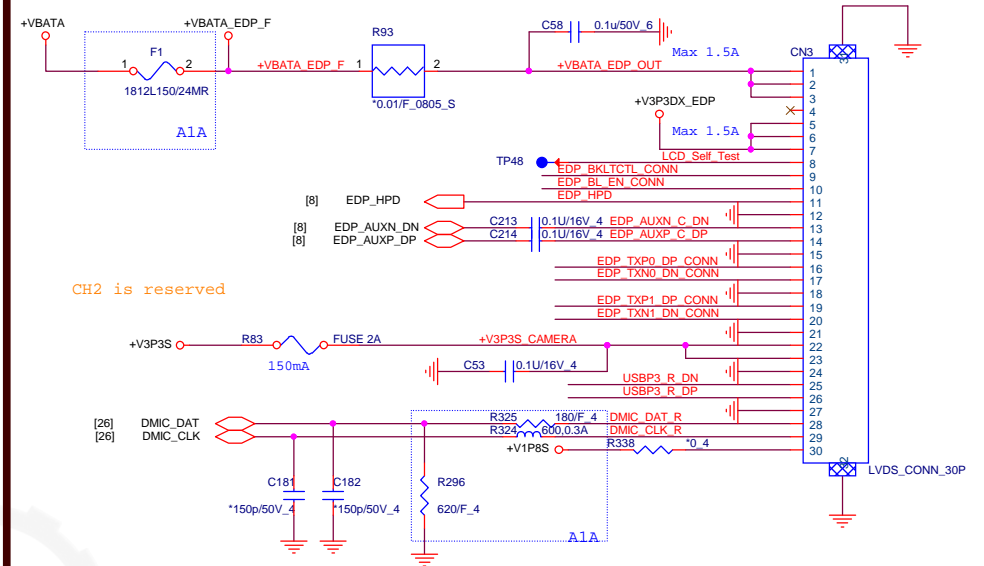


eDP Power



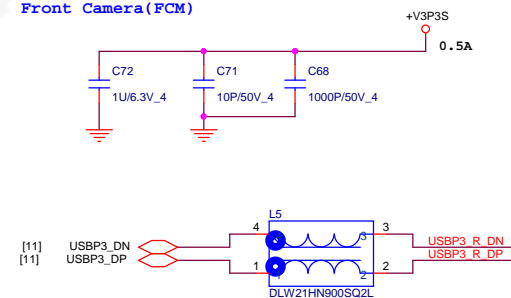
eDP CONNECTOR

LCD(LDS)

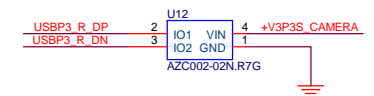


CAMERA - POWER AND USB CMC

Front Camera(FCM)



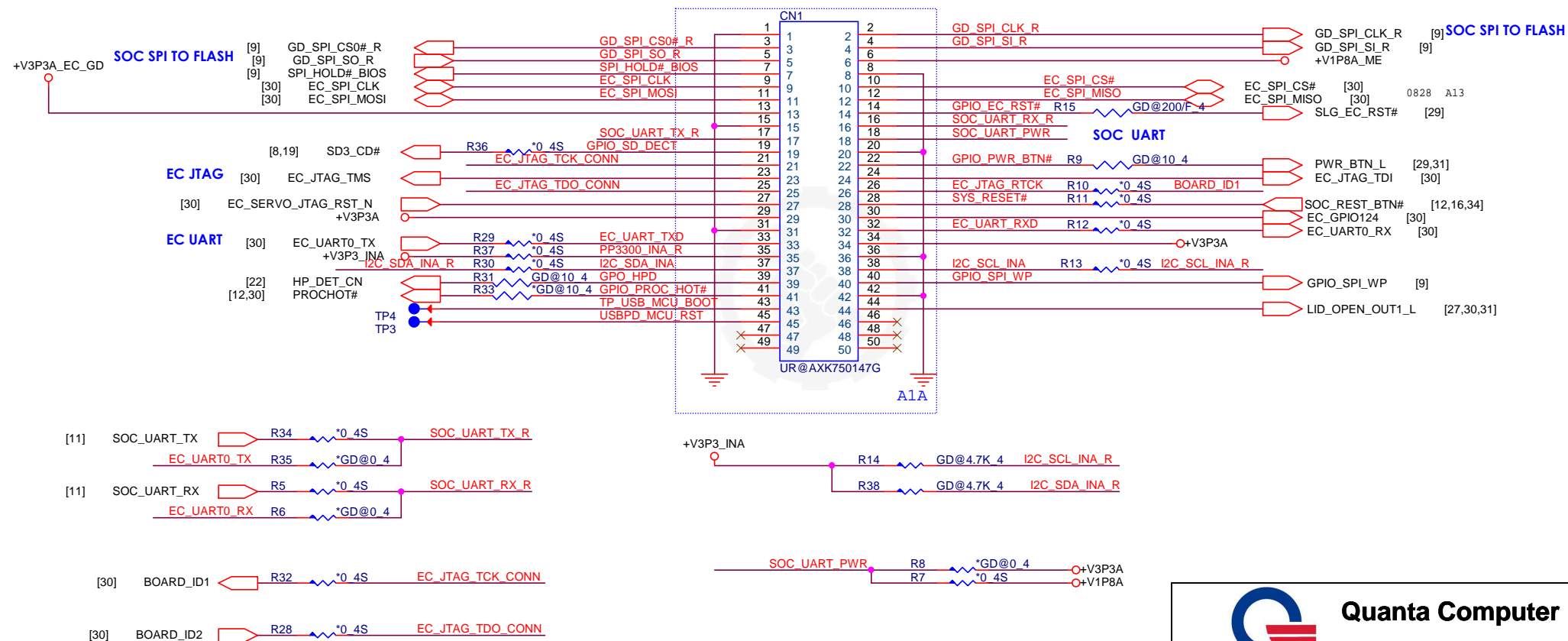
ESD



Layout note: Place close to CN9

Vinafix.com

PIN7 OD	PIN39 OD	PIN49 OD
PIN14 OD	PIN41 OD	PIN50 OD
PIN19 OD	PIN43 OD	
PIN22 OD	PIN44 OD	
PIN28 OD	PIN45 OD	
PIN30 OD	PIN46 OD	
PIN37 OD	PIN47 OD	
PIN38 OD	PIN48 OD	



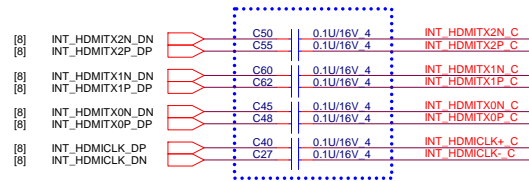
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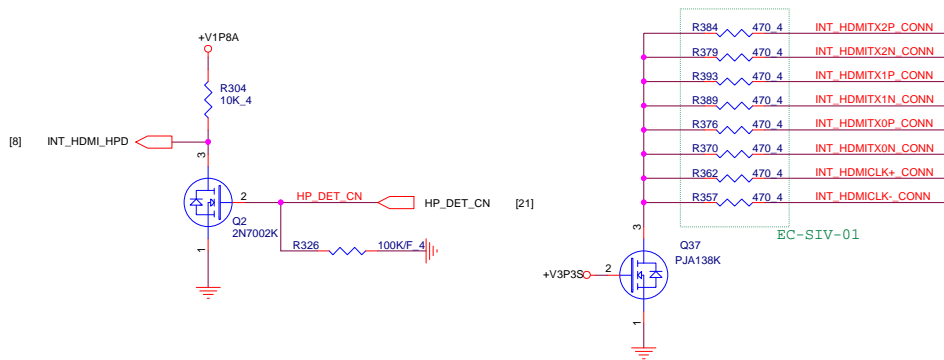
Size	Document Number	Rev
	Google Debug	A1A
Date:	Monday, December 12, 2016	Sheet 21 of 44

HDMI LEVEL SHIFTER

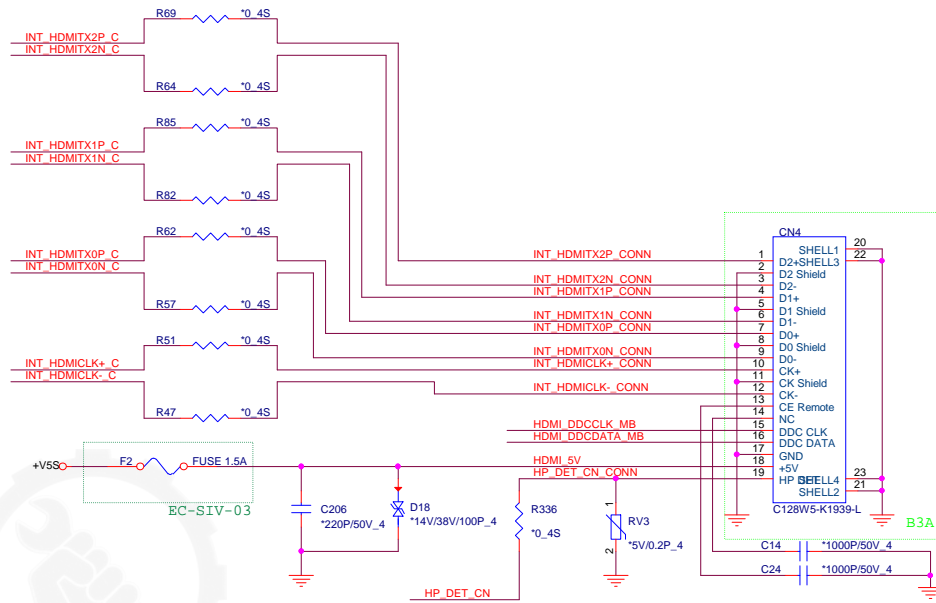
Vinafix.com



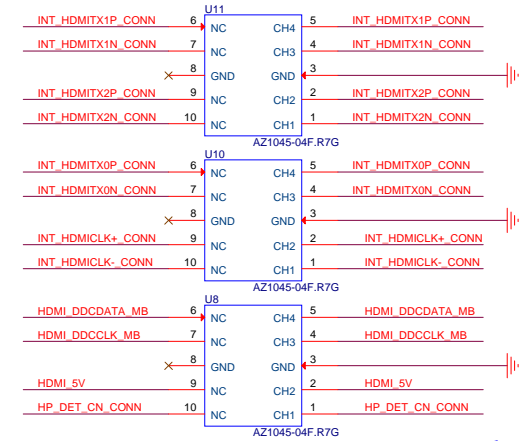
Layout Notes:
Place decoupling CAPs
close to Connector



HDMI CONNECTOR



ESD 靠近HDMI CONNECTOR(CN2)

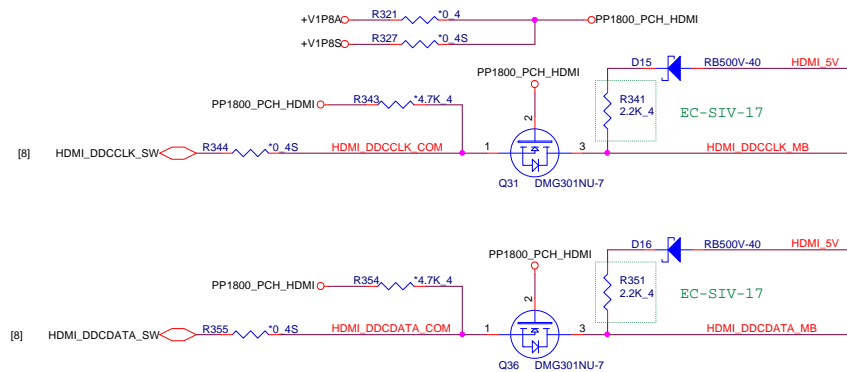


For ESD

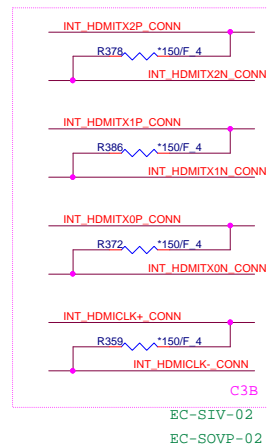
Layout note: Place close to HDMI Conn

EC-DV-11

LEVEL TRANSLATOR/ EMI



EMI



EC-SIV-02
EC-SOVP-02

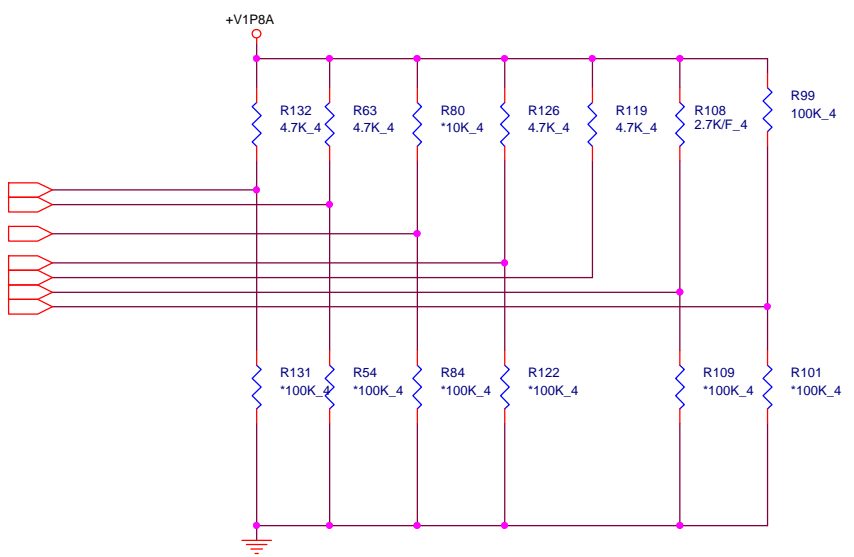
SoC (CPU)

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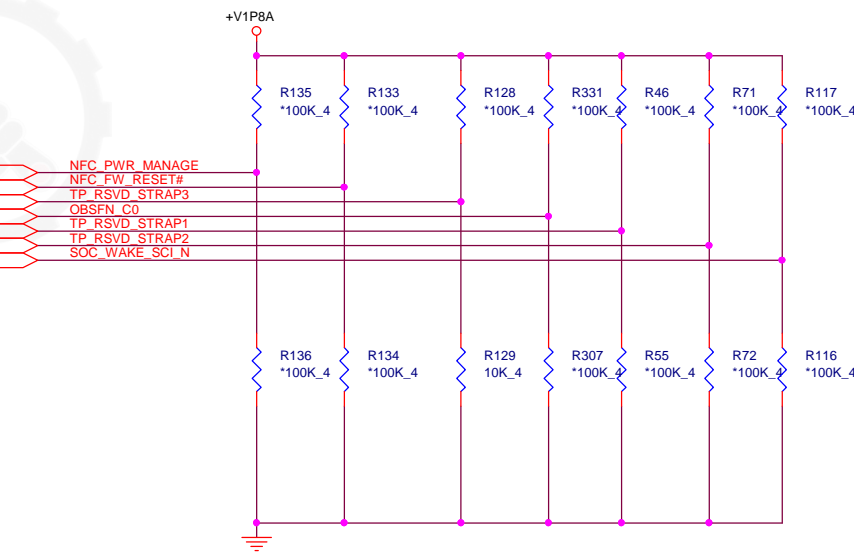
BSW Strapping Table (based on EDS V1.0), sampled on the rising edge of PMU_RSMRST_N

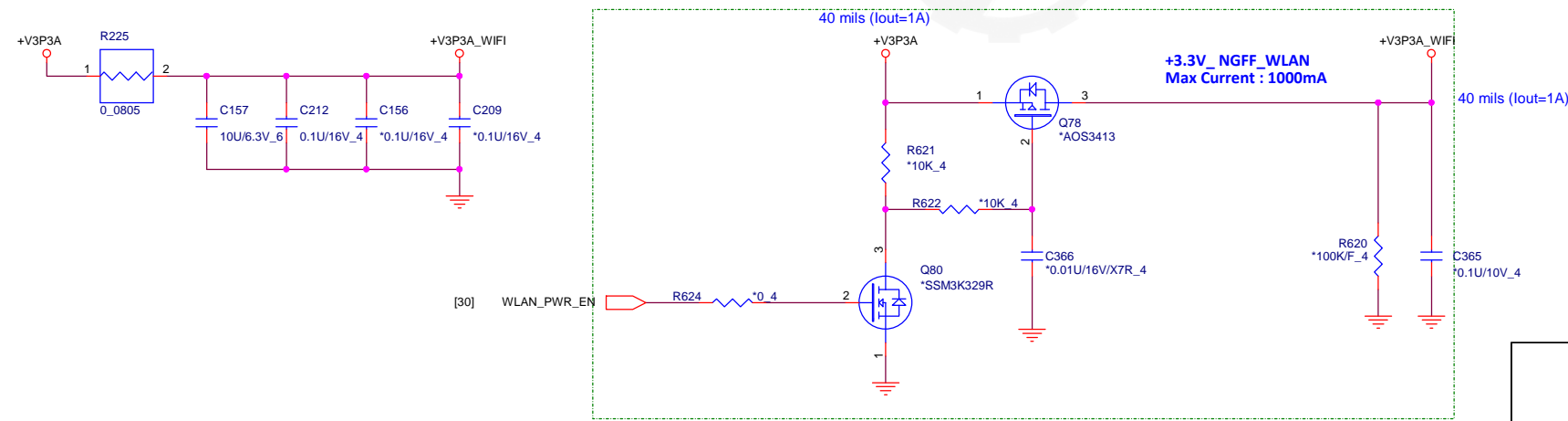
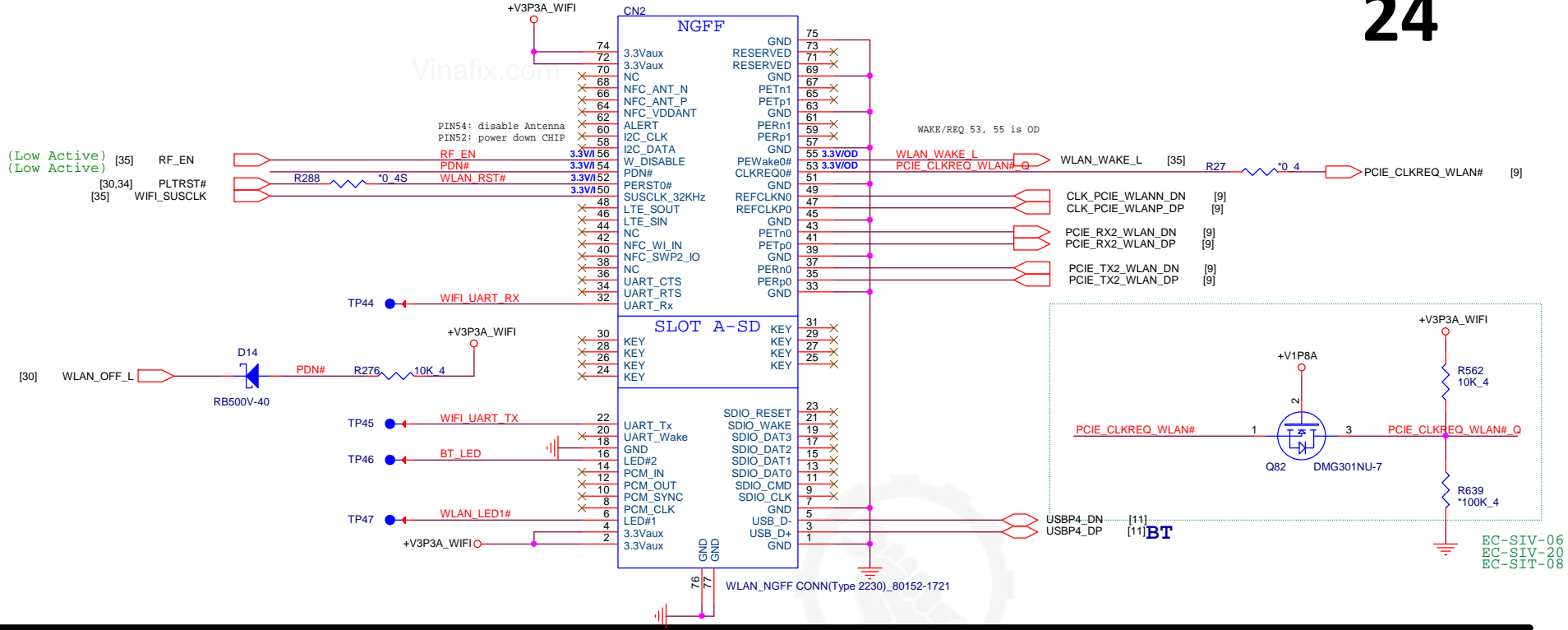
Pin Name	Strap description	Configuration
GPIO_SUS0	DDI0 Detect	0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS1	DDI1 Detect	0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS2	Top Swap (A16 Override)	0 = change boot loader address 1 = Normal operation
GPIO_SUS3	DSI Display Detect (Leave floating if GPIO functionality is not used, it is not POR)	0 = DSI not detected 1 = DSI detected
GPIO_SUS4	BIOS Boot Selection	0 = No SPI 1 = SPI
GPIO_SUS5	Security Flash Descriptors	0 = Not support 1 = Normal operation
GPIO_SUS6	Halt Boot strap	1 = Normal operation (MUST be high at RSMRST# de-assert to ensure proper platform operation and use of GPIO_DFX[8:0])
GPIO_SUS7	DFX SUS DEBUG strap	0 = SUSDUG 1 = No SUSDUG
GPIO_SUS8	PLLs,ICLK,USB2,DDI ,SFR,supply select	0 = Supply is 1.25V 1 = Supply is 1.35V
GPIO_SUS9	ICLK,USB2,DDI,SFR Bypass	0 = No Bypass(Default) 1 = Bypass with 1.05V
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	0 = No Bypass(Default) 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	0 = No Bypass(Default) 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	0 = No Bypass(Default) 1 = Bypass

[10,35] MUX_AUD_INT1#
[10,34] EC_SML_L
[10,34] KBD_IRQ#
[10,29] TRACKPAD_INT#
[10] EC_KBD_ALERT_SOC
[10,16] SOC_RUNTIME_SCI
[10] SOC_KBC_SMI



[10] NFC_PWR_MANAGE
[10] NFC_FW_RESET#
[10] TP_RSVD_STRAP3
[8,16] OBSFN_C0
[8] TP_RSVD_STRAP1
[8] TP_RSVD_STRAP2
[10,34] SOC_WAKE_SCI_N





LTE NGFF Power(LTE)


25

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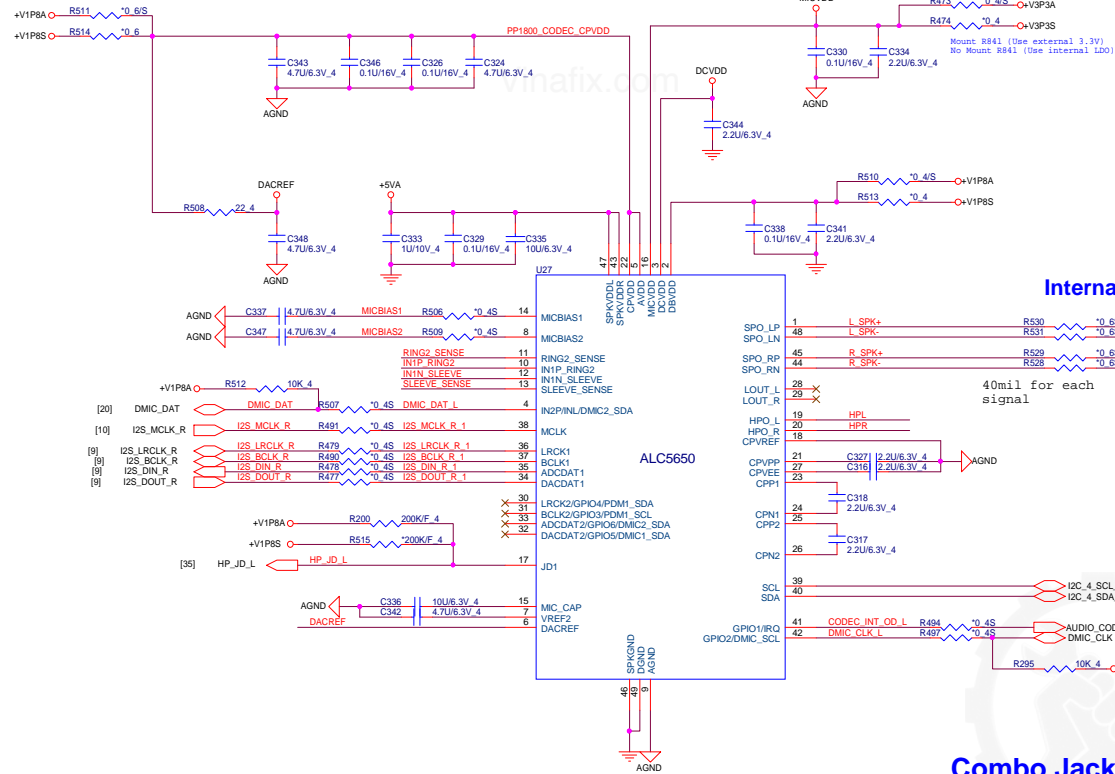
Removed (2015/03/27)

LTE NGFF (LTE)

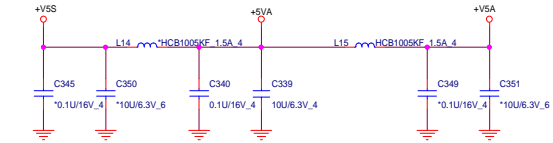


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		PROJECT : ZHM	
Size	Document Number	Rev	
	LTE(NGFF)	A1A	
Date: Monday, December 12, 2016		Sheet	25 of 44

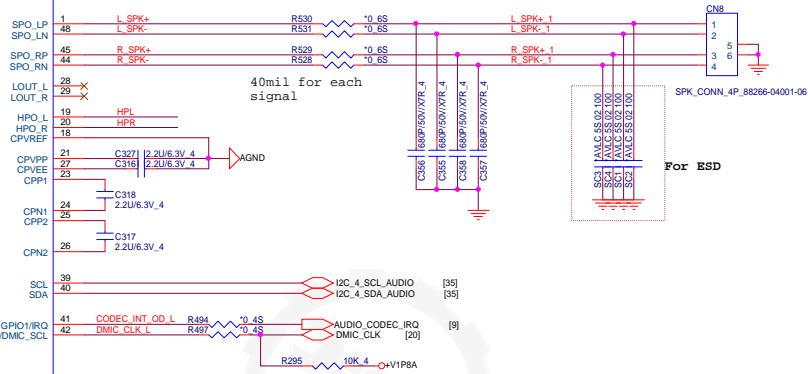
Codec (ADO)



Codec PWR 5V (ADO)



Internal Speaker (ADO)



Combo Jack (ADO)

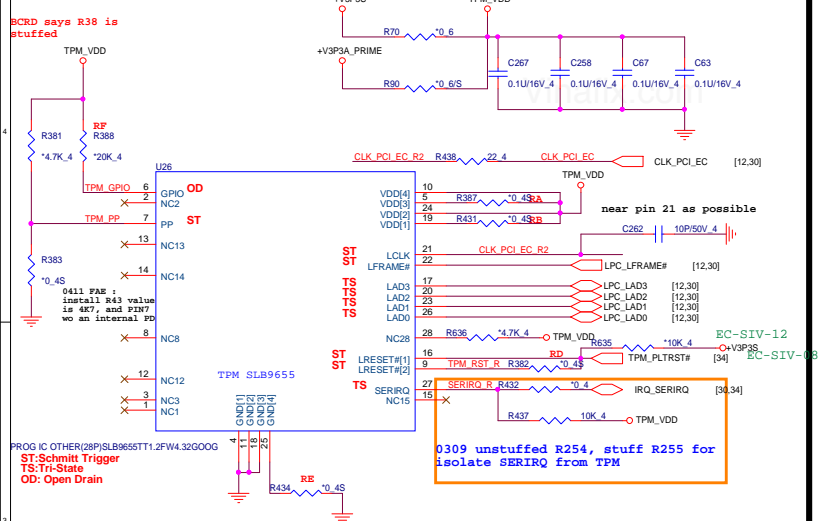


To be validated if ESD protections are un-stuffed

TPM/DAUGHTER BOARD CONNECTOR

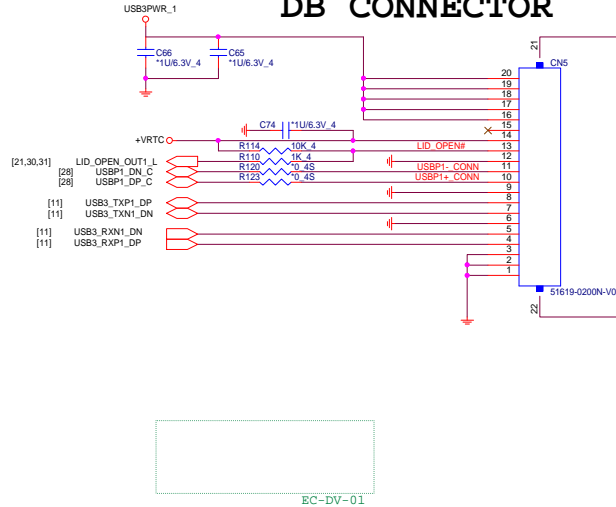
TPM(TPM)

TPM

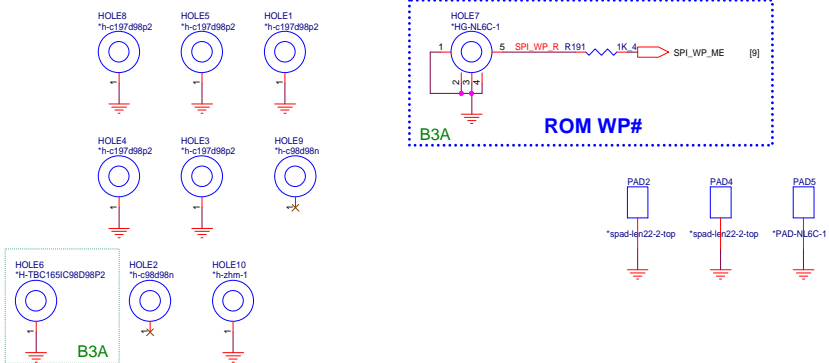


DB(UIF)

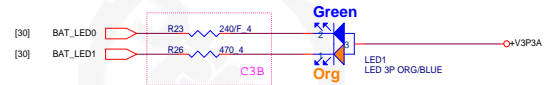
DB CONNECTOR



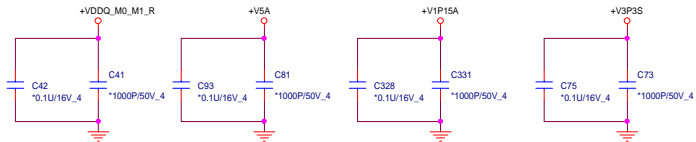
Holes(OTH) MOUNTING HOLES



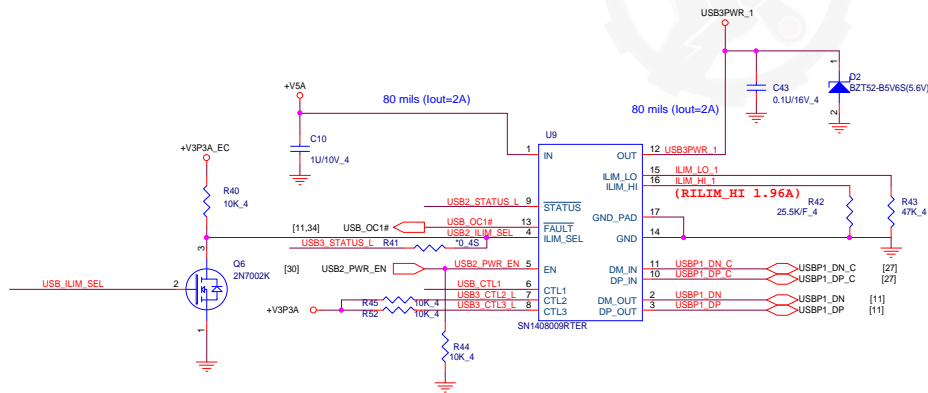
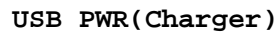
Battery LED

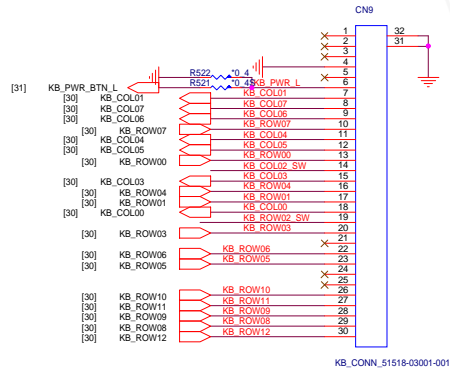


EMI caps

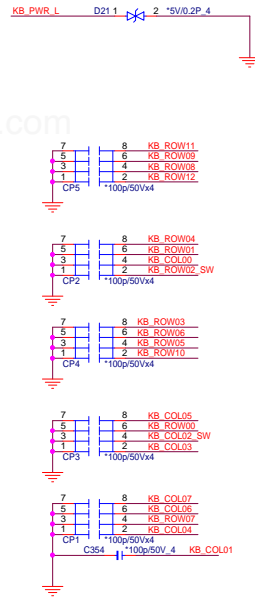


RF caps



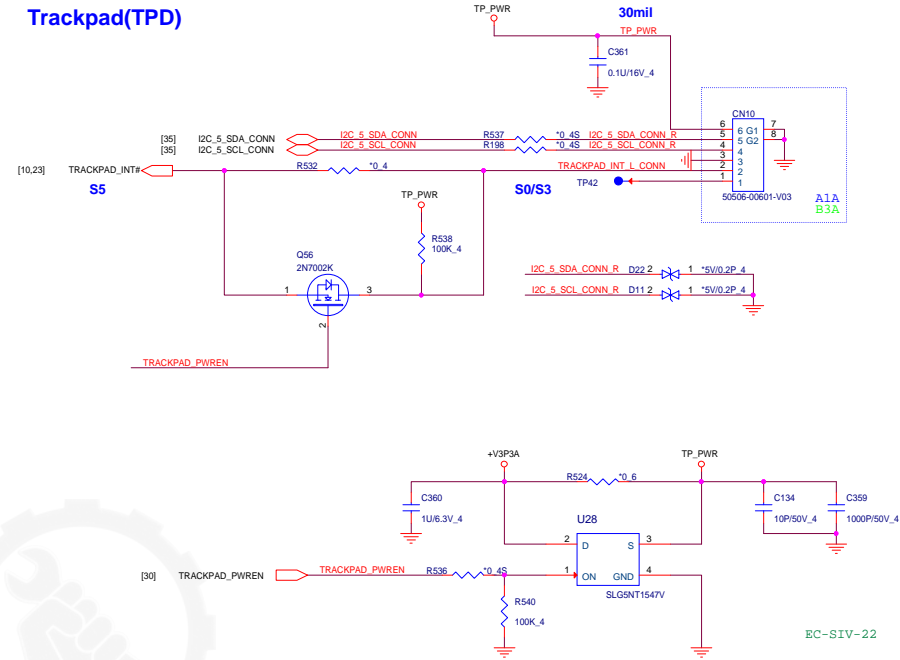


Vinafix.com



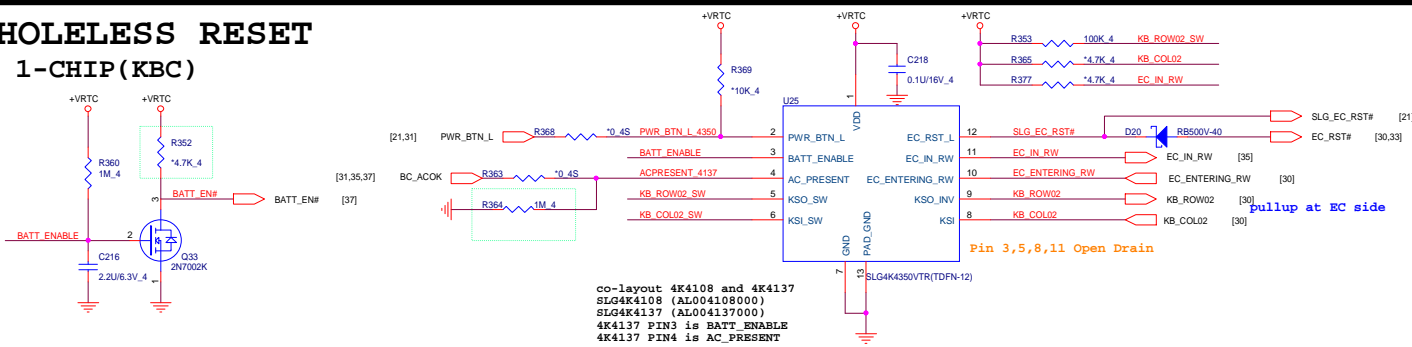
TRACK PAD BOARD CONN

Trackpad(TPD)



HOLELESS RESET

1-CHIP(KBC)

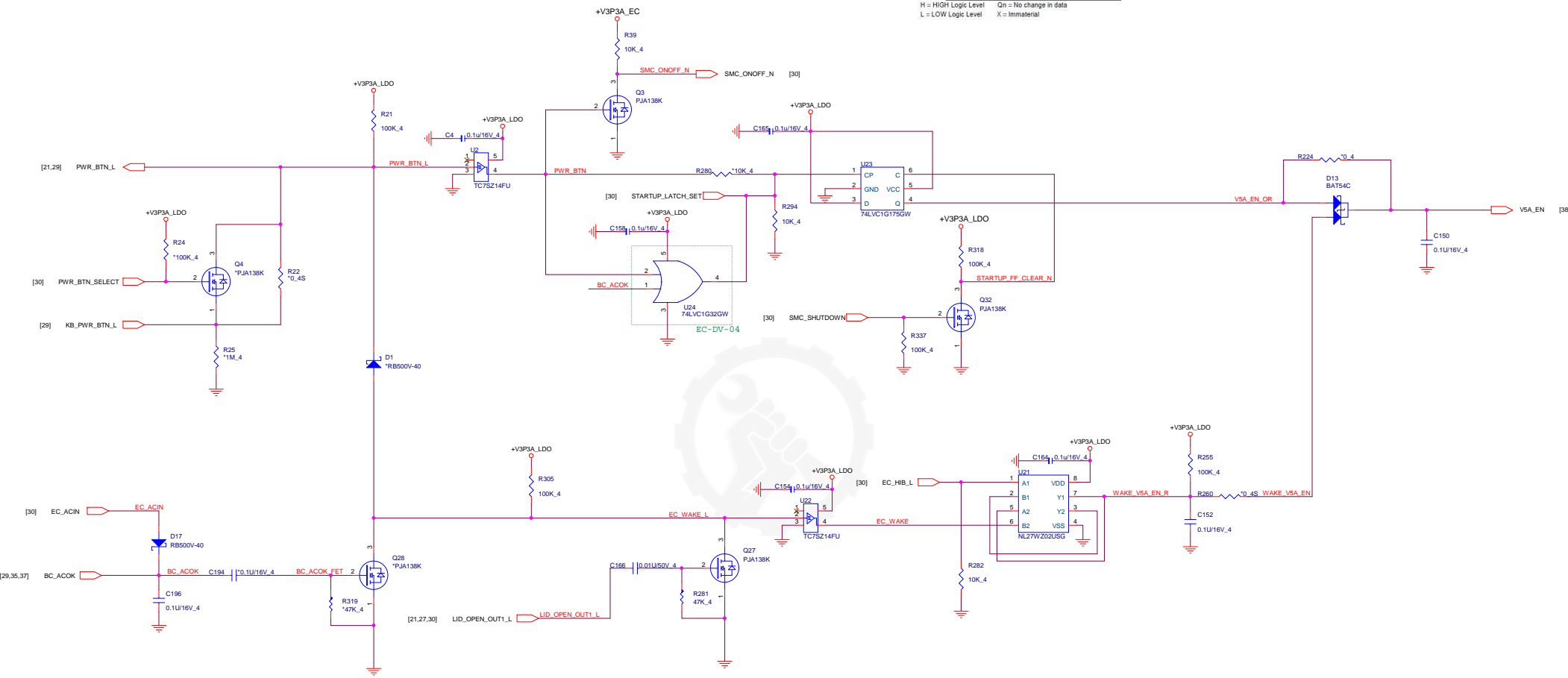


Vinafix.com

Function Table

Inputs		Output	
CP	D	C	Q
✓	L	H	L
✓	H	H	H
✓	X	H	Qn
X	X	L	L

H = HIGH Logic Level
L = LOW Logic Level
Qn = No change in data
X = Immaterial



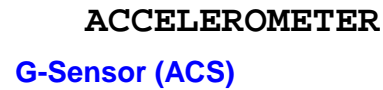
EC HIB WAKE SOURCES

Removed (2015/03/30)

Vinafix.com



THERMAL SENSOR



Removed (2015/03/27)

Touch screen(TSN)

Removed (2015/03/27)

Removed (2015/03/27)

LED board(UIF)

Removed (2015/03/27)



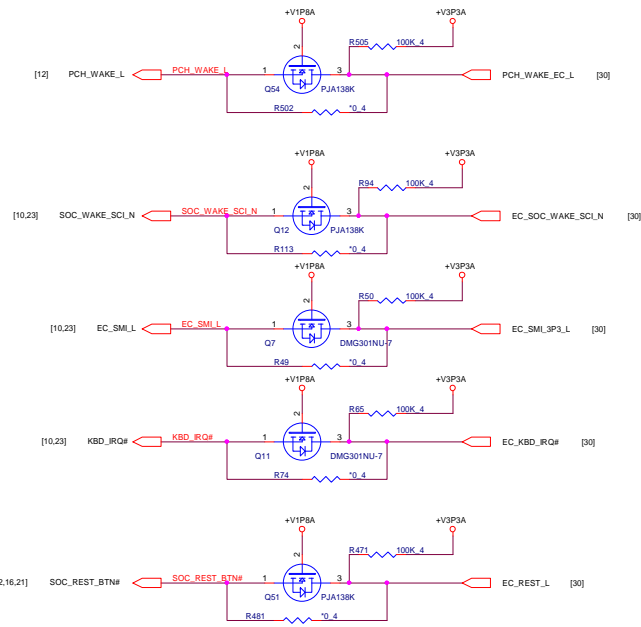
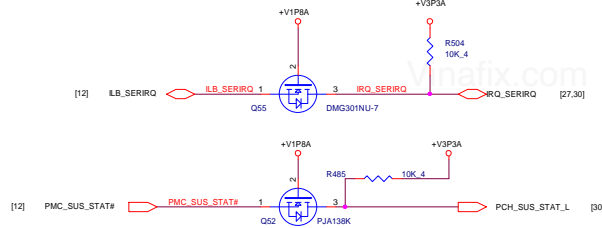
PROJECT : ZHM

SENSORS

Size	Document Number	Rev
	SENSORS	A1A
Date:	Monday, December 12, 2016	Sheet 33 of 44

SoC(CPU)

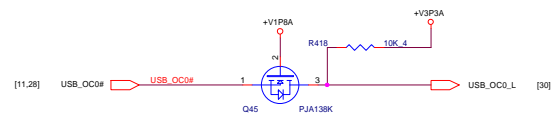
PWRON SEQUENCE



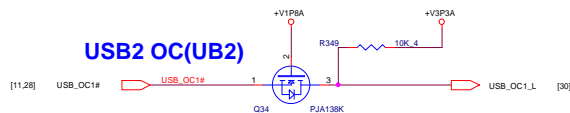
0311 Added 5 FETs as level shifters on EC OD GPIOs

USB OC

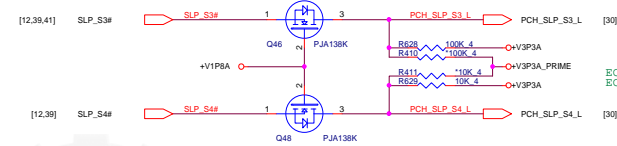
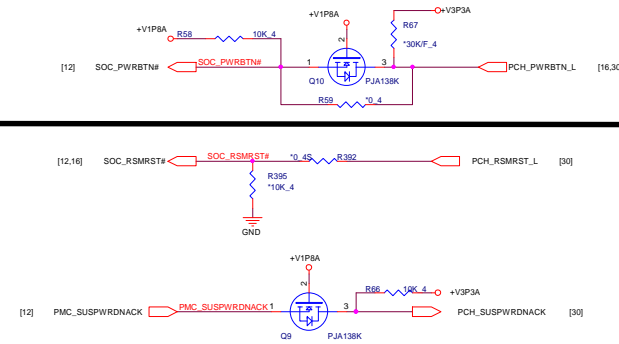
USB3 OC(UB3)



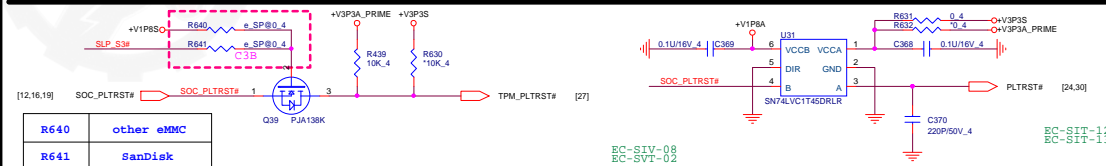
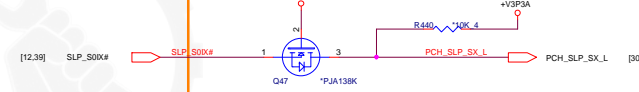
USB2 OC(UB2)



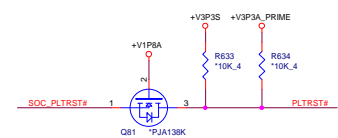
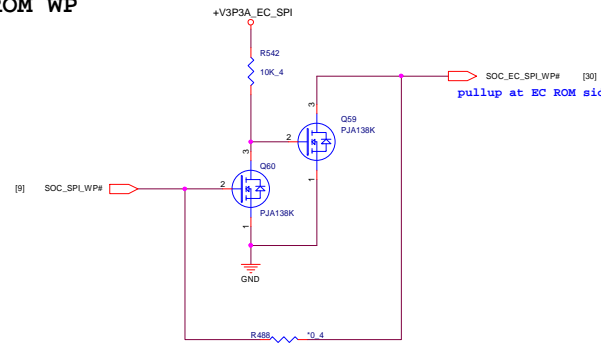
PWRON SEQUENCE



0305 SLP_SX related components are stuffed



ROM WP



LTE(LTE)

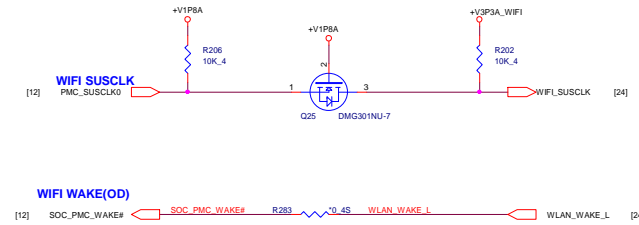
Removed (2015/03/27)

Vinafix.com

WiFi(NGF)

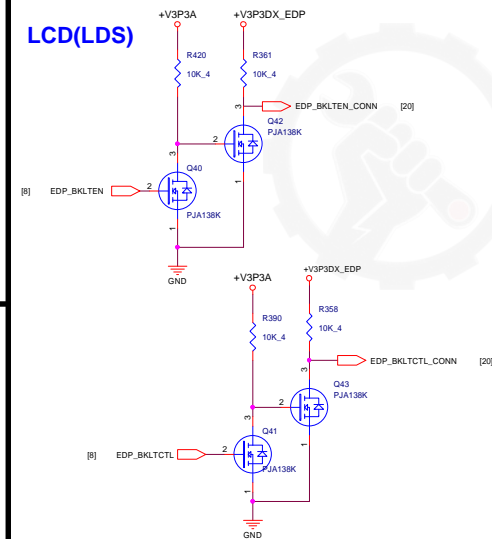
LEVEL TRANSLATOR 2

WIFI SIGNALS



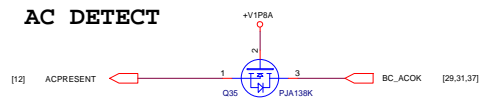
eDP CONTROL PIN

LCD(LDS)

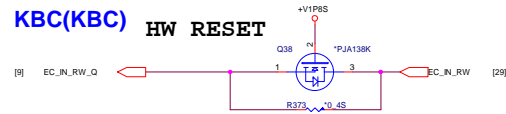


KBC(KBC)

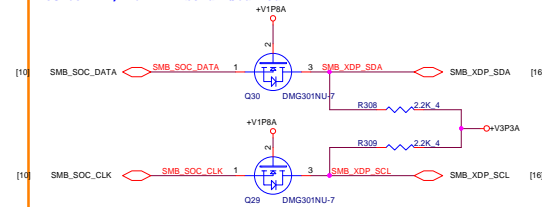
AC DETECT



KBC(KBC) HW RESET

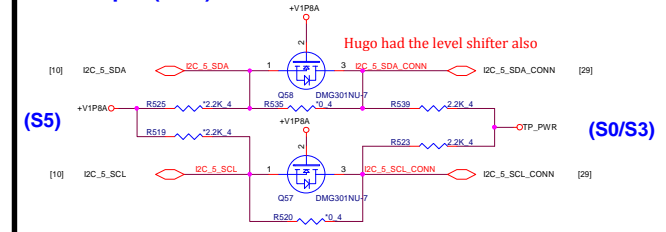


0310 Added level shifter on SMBUS from soc to XDP, it will be un-stuffed in MP



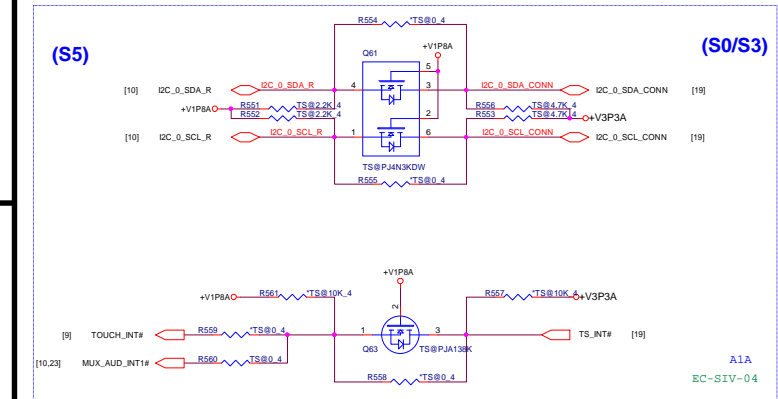
TRACK PAD I2C_5 SIGNALS

Trackpad(TPD)

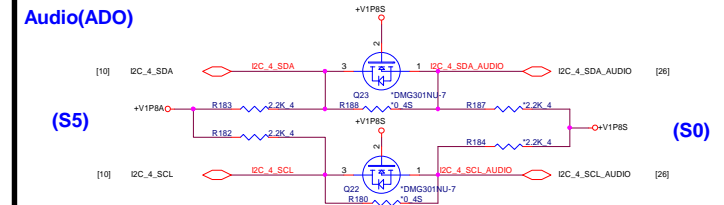


Touch Screen(TSN)

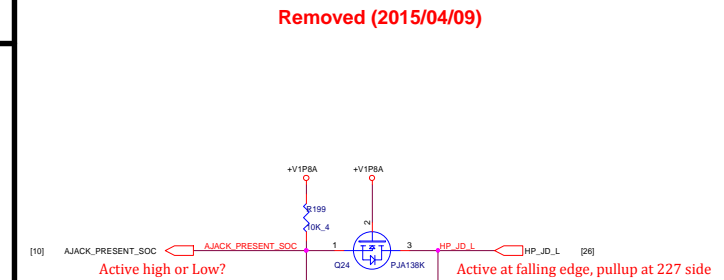
TOUCH SCREEN I2C_0 SIGNALS



Audio(ADO)

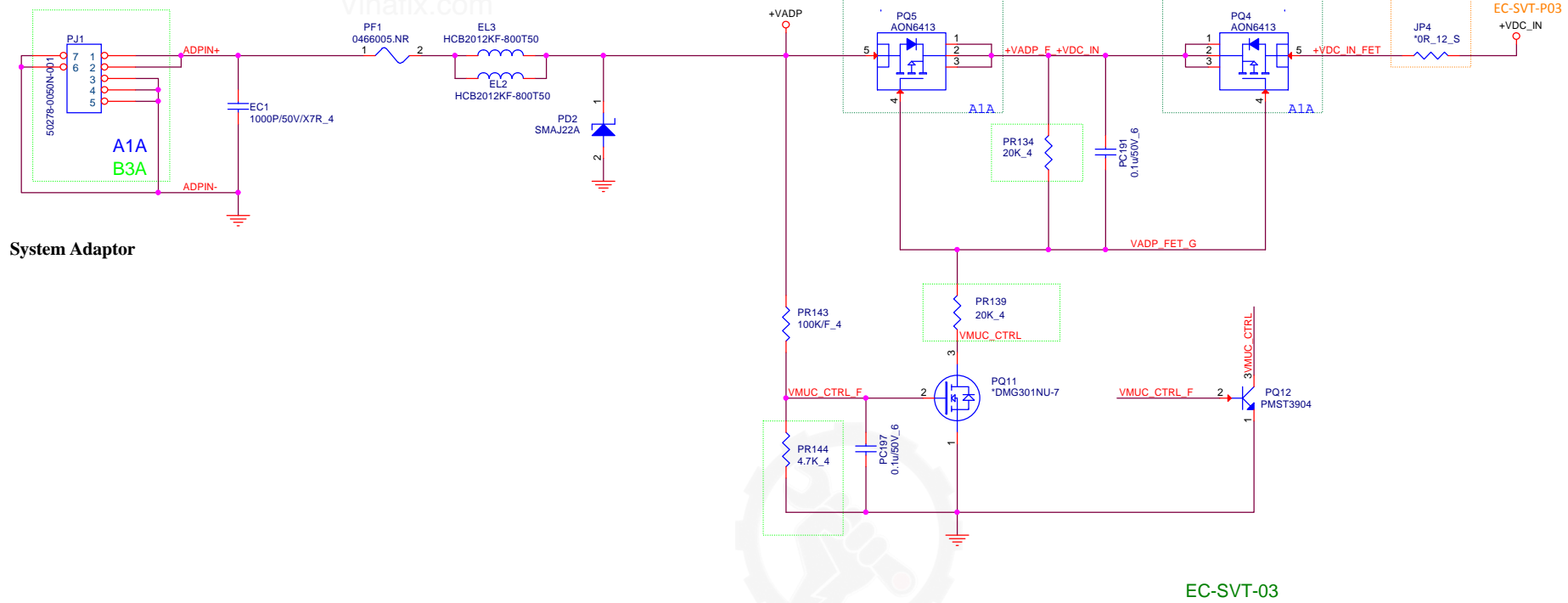


Removed (2015/04/09)



DC JACK

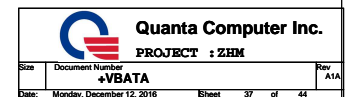
36

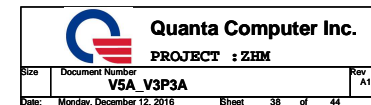


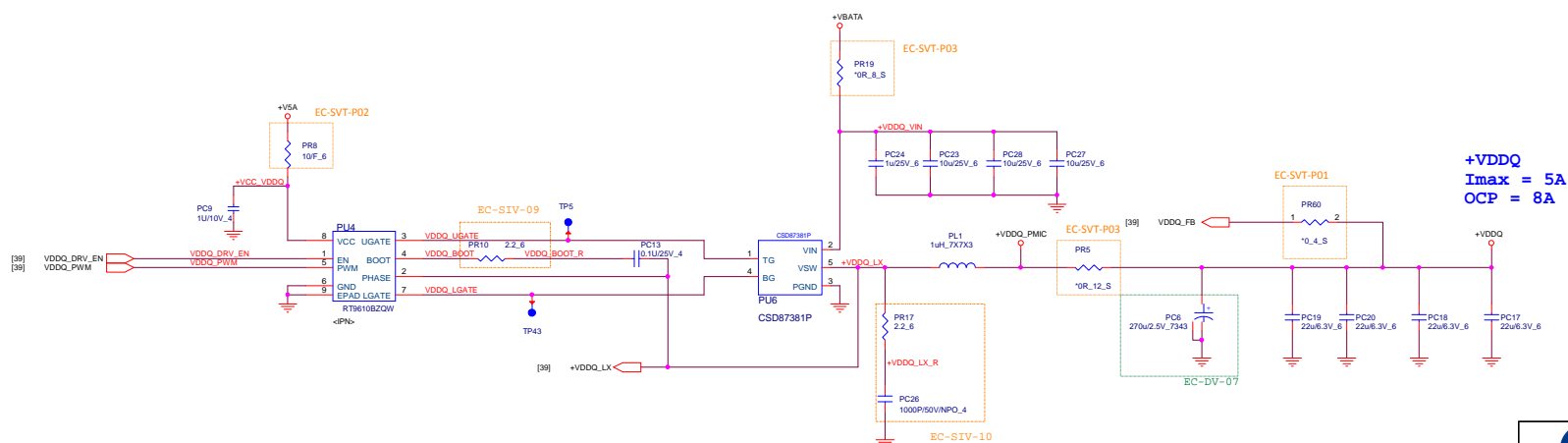
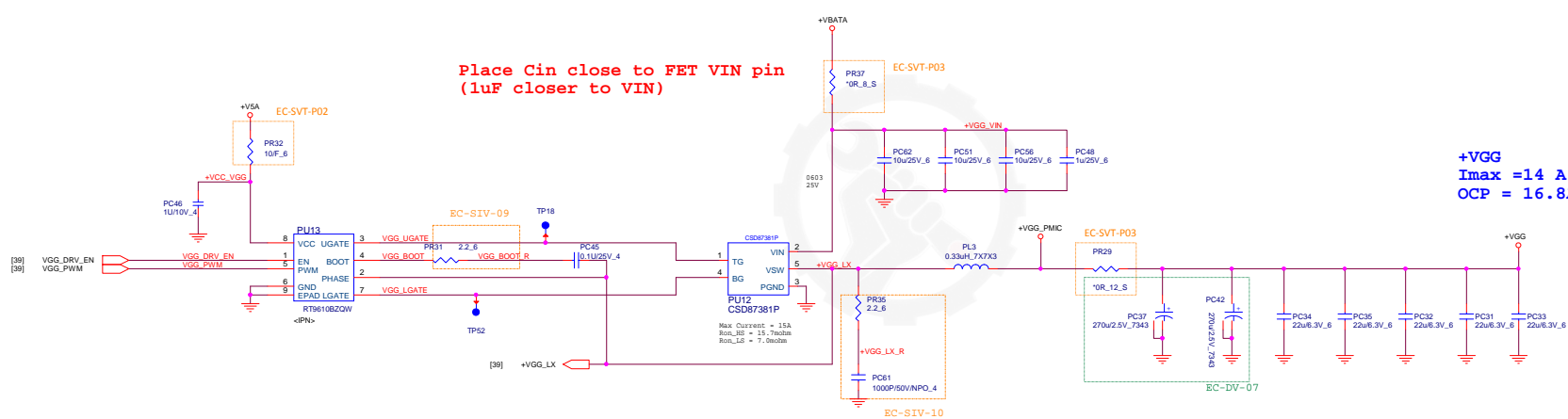
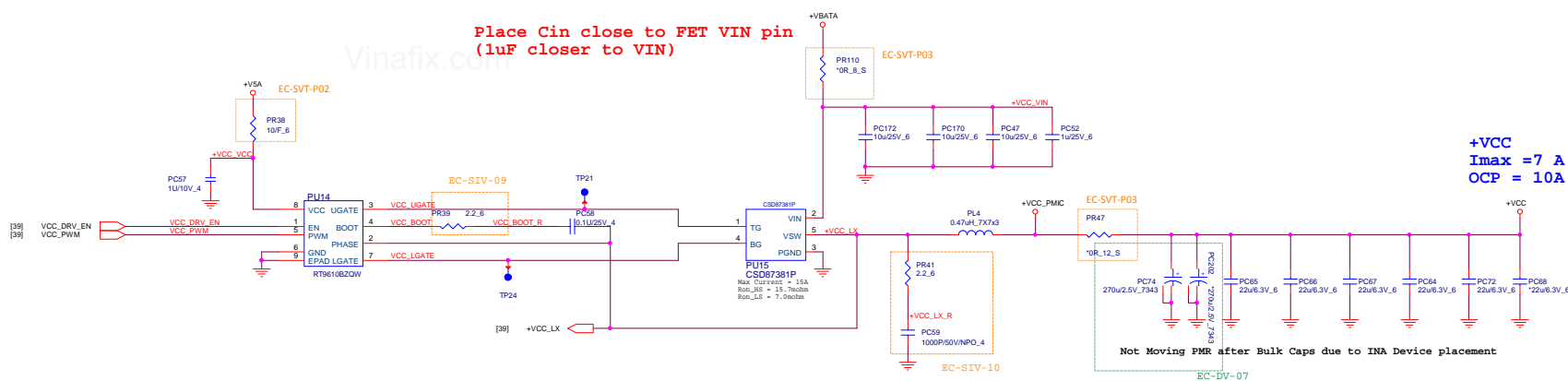
EC-SVT-03



BATTERY CONNECTOR

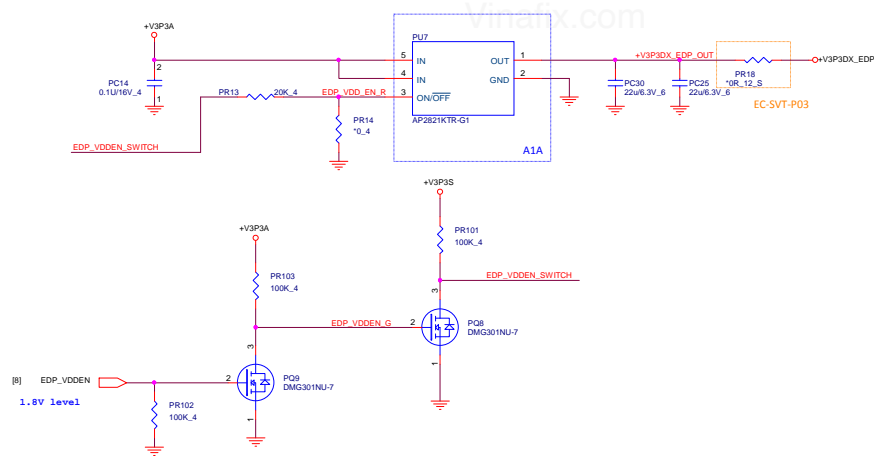




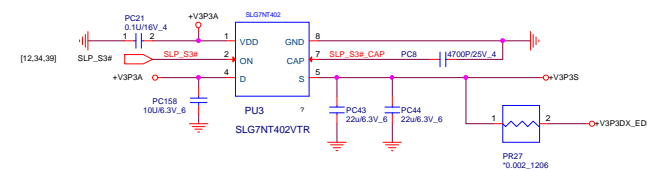


+V3P3DX_EDP: VCC_EDP

CHECK SLEW RATE



DEFAULT OPTION FOR PANEL POWER SEQUENCING

+V3P3S

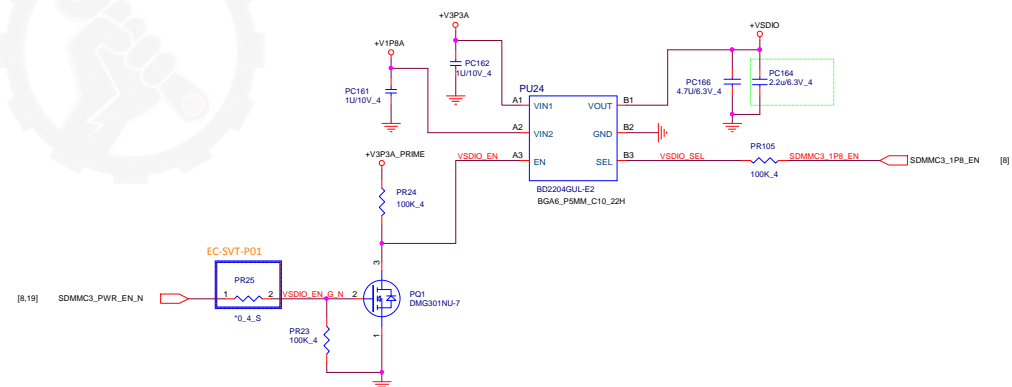
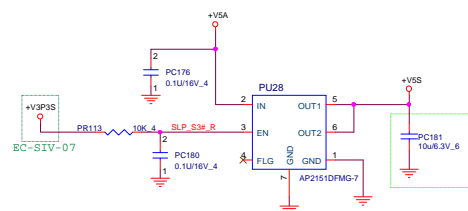
Notes:
Imax: 4A
Rise time: 1ms

+VSDIO

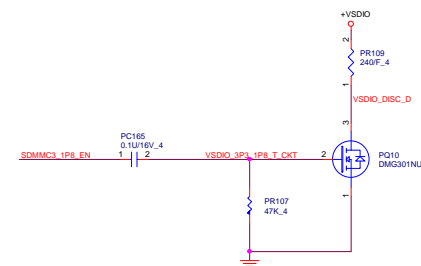
SDMMC3_PWR_EN_N	SDMMC3_1P8_EN	VSDIO_V
0	0	0V
1	0	0V
0	1	3.3V
0	1	1.8V

Notes:
Imax: 100 mA
Rise time: 150 uSec

CAD Note : place the caps close to IC
 NEW FOOT PRINT IS REQUIRED

**+V5S**

Design Note :
 controls the time when VSDIO changes from 3.3V to 1.8V



ZHM Schematic EC Tracking Record A

[illegible]

ZHM Schematic EC Tracking Record A1A to C version

[illegible]

ZHM Schematic EC Tracking Record C to MP version

[illegible]